Discrete/UMA /Muxless Schematics Document

AMD LIANO CPU FS1

AMD GPU Manhattan(Park/Madison M2) and Vancouver(Seymour/Whistler M2)

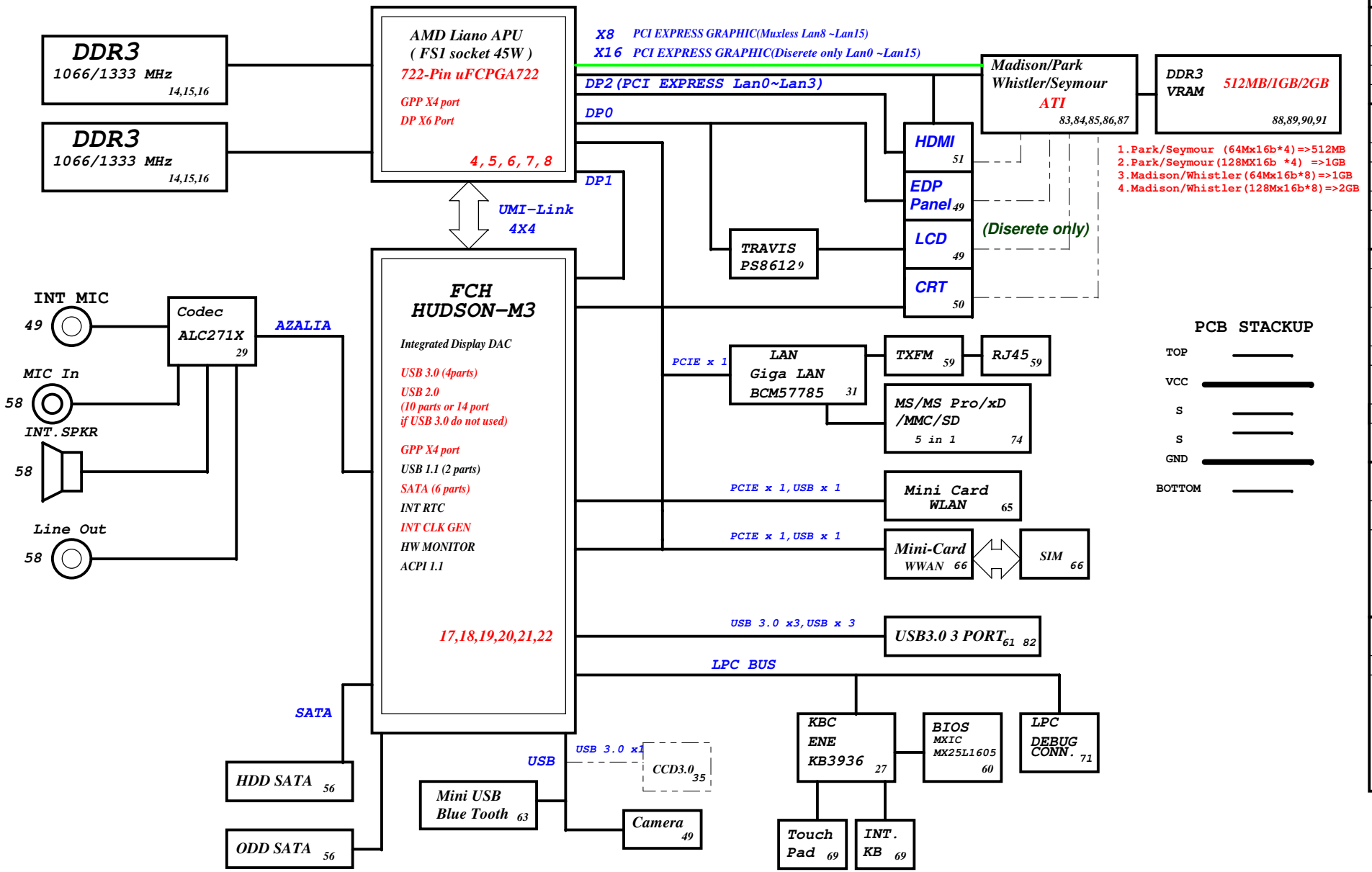
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A4	Document Number: JE50_SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 1 of 102	

JE50-SB Block Diagram

JE50-SB Project code:91.4M701.001



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8239 — 41

INPUTS	OUTPUTS
DCBATOUT	5V_S5(5.5A) 3D3V_S5(5A)

SYSTEM DC/DC RT8207 — 44

5V_S5	1D5V_S3(15A)

RT8207 — 44

5V_S5	0D75_S0(1.2A)

SYSTEM DC/DC RT8238 — 46

INPUTS	OUTPUTS
5V_S5	1D1V_S5(1.4A)

RT8238 — 45

5V_S5	1D2V_S0(5.2A)

RT9025 — 93

3D3V_S5	1D8V_VGA_S0
1D5V_S3	1V_VGA_S0

RT9025 — 48

3D3V_S0	2D5V_S0 (200mA)

RT8208 — 92

5V_S5	VGA_CORE

CHARGER BQ24745 — 40

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6267 — 42,43

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.55V 18A VDDNB 0~1.55V 4A

<Variant Name>

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Title: Block Diagram

Size: A3 | Document Number: JE50_SB | Rev: SB

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Strapping

REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USB Table

USB	
Pair	Device
0	USB 2.0 EXT2(For SW Debug)
1	WLAN
2	NC
3	WWAN
4	BT
5	3G SIM Card
6	NC
7	CCD
8	NC
9	Card Reader
10	USB 3.0 port 1
11	USB 2.0 EXT2
12	USB 2.0 EXT3
13	NC

PCIE Routing

	APU
LANE0	LAN
LANE1	WWAN
LANE2	LAN
LANE3	

	FCH
LANE0	
LANE1	
LANE2	
LANE3	

<Variant Name>

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Size: A3 | Document Number: JE50_SB | Rev: SB

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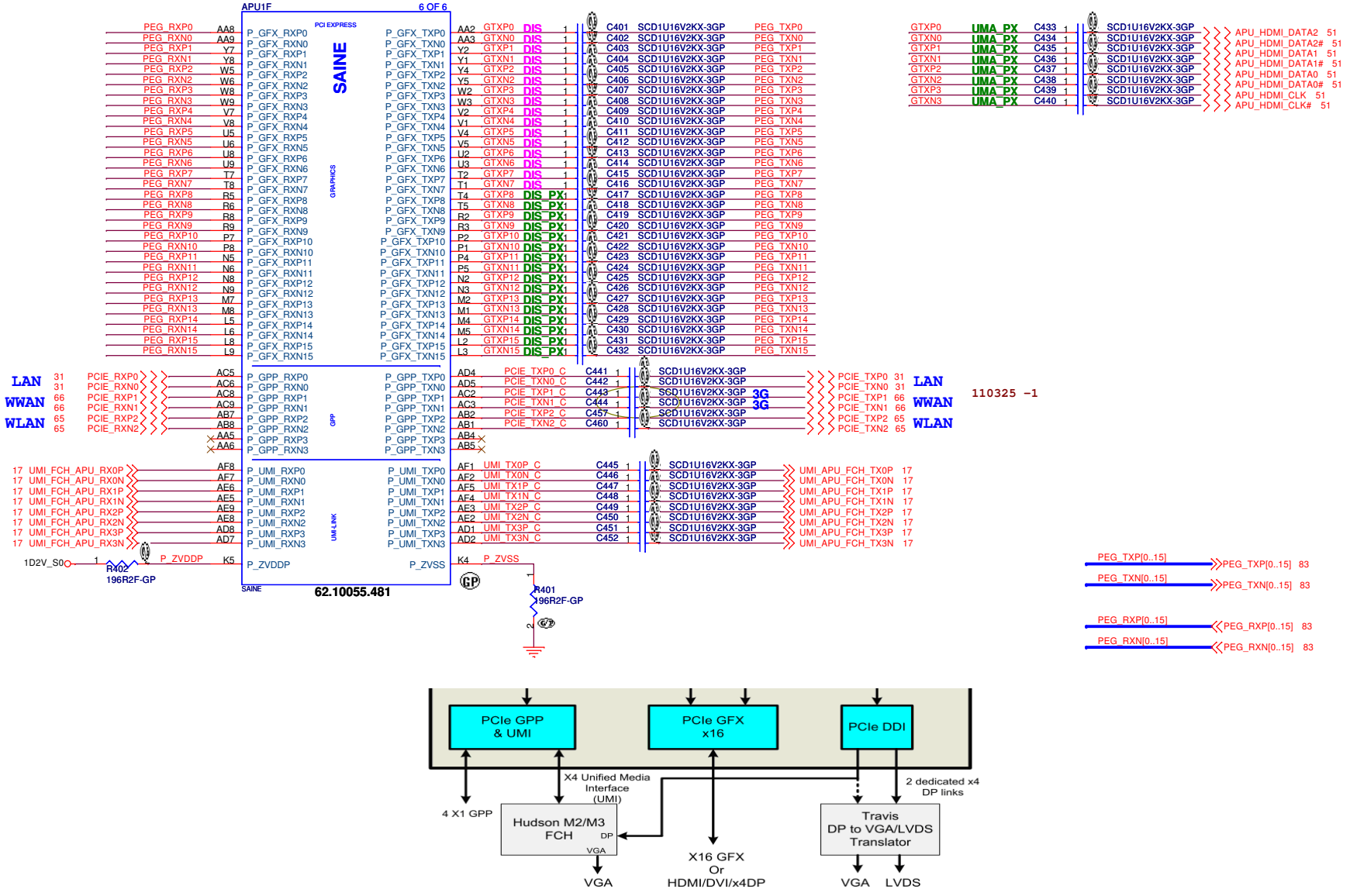

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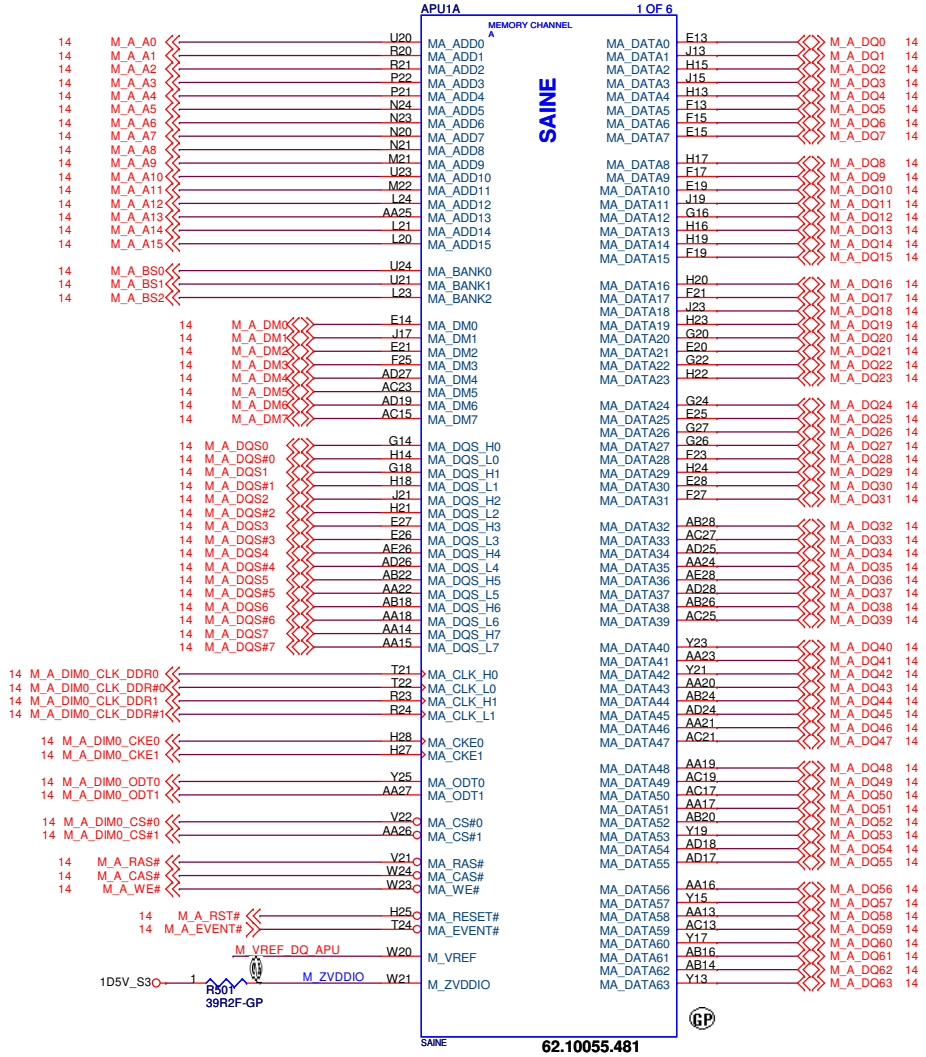
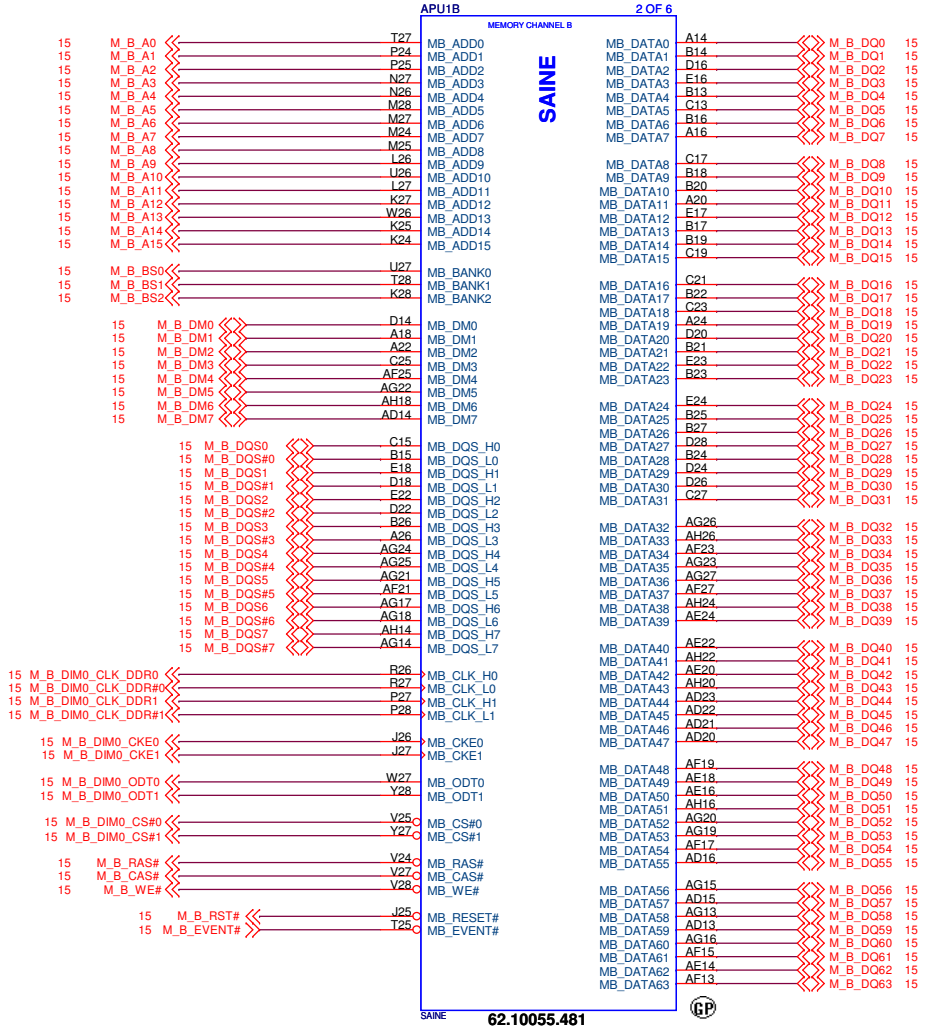
Title: APU_PCIE(1/5)

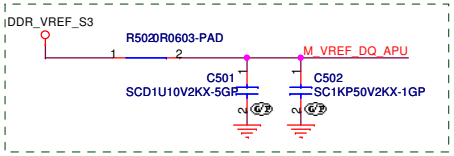
Size	Document Number	Rev
A3	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 4 of 102

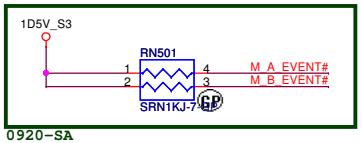




APU_VREF_DQ



LAYOUT: place them close to APU



0920-SA

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Title: APU_DDR(2/5)

Size	Document Number	Rev
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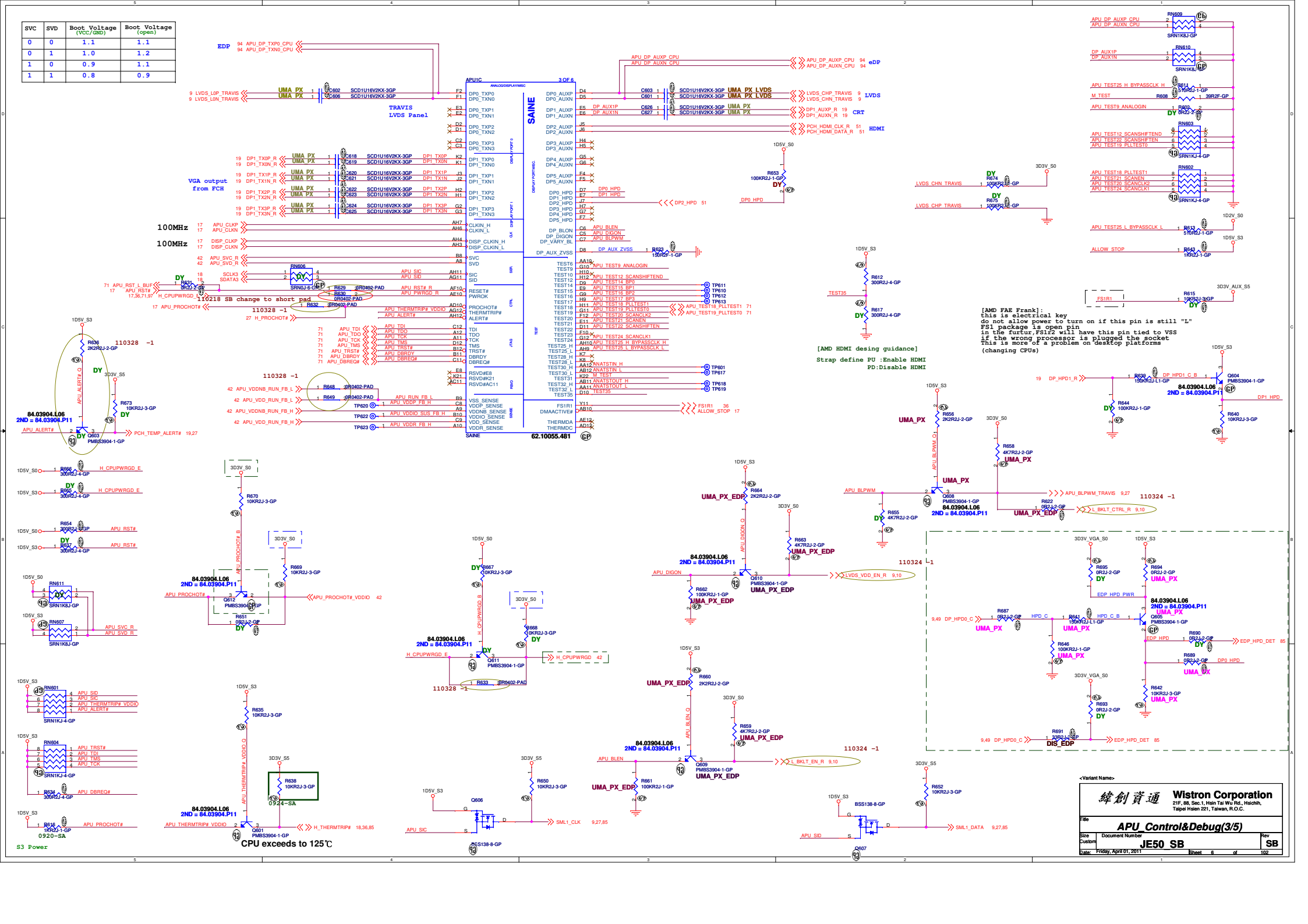
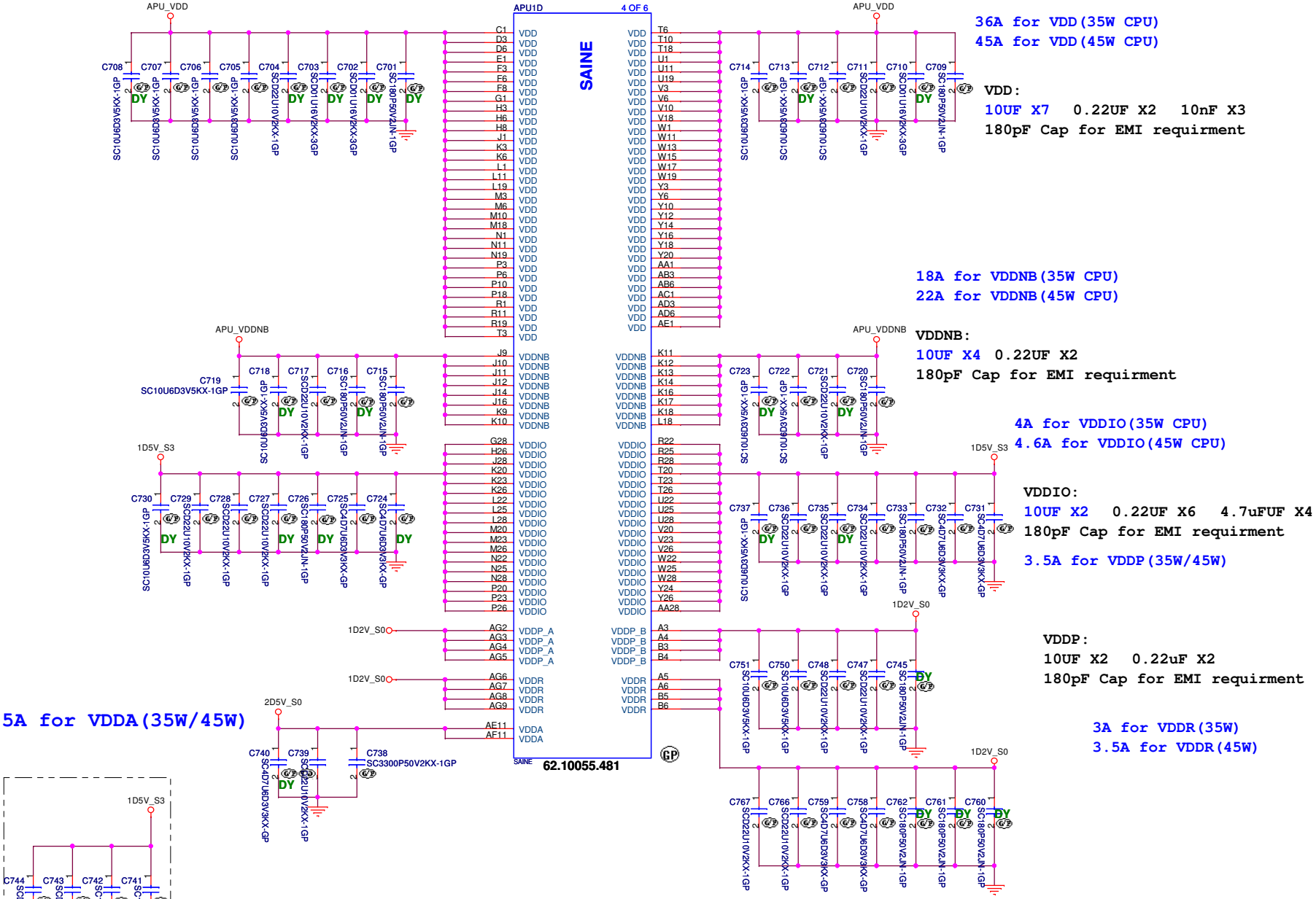
SVC	SVD	Boot Voltage (VCC/GND)	Boot Voltage (open)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.1
1	1	0.8	0.9





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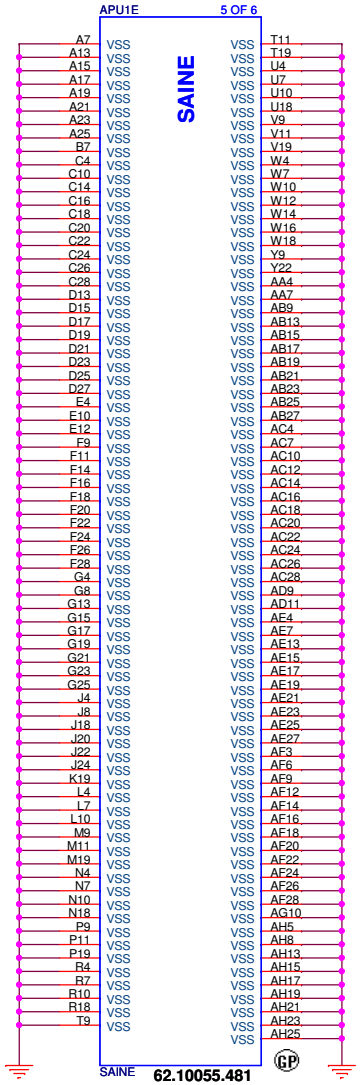
<variant_name>

Title: APU_Power(4/5)

Size: A3 | Document Number: JE50_SB | Rev: SB

Date: Friday, April 01, 2011 | Sheet 7 of 102



<Variant Name>

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Title: APU_VSS(5/5)

Size	Document Number	Rev
A3	JE50_SB	SB

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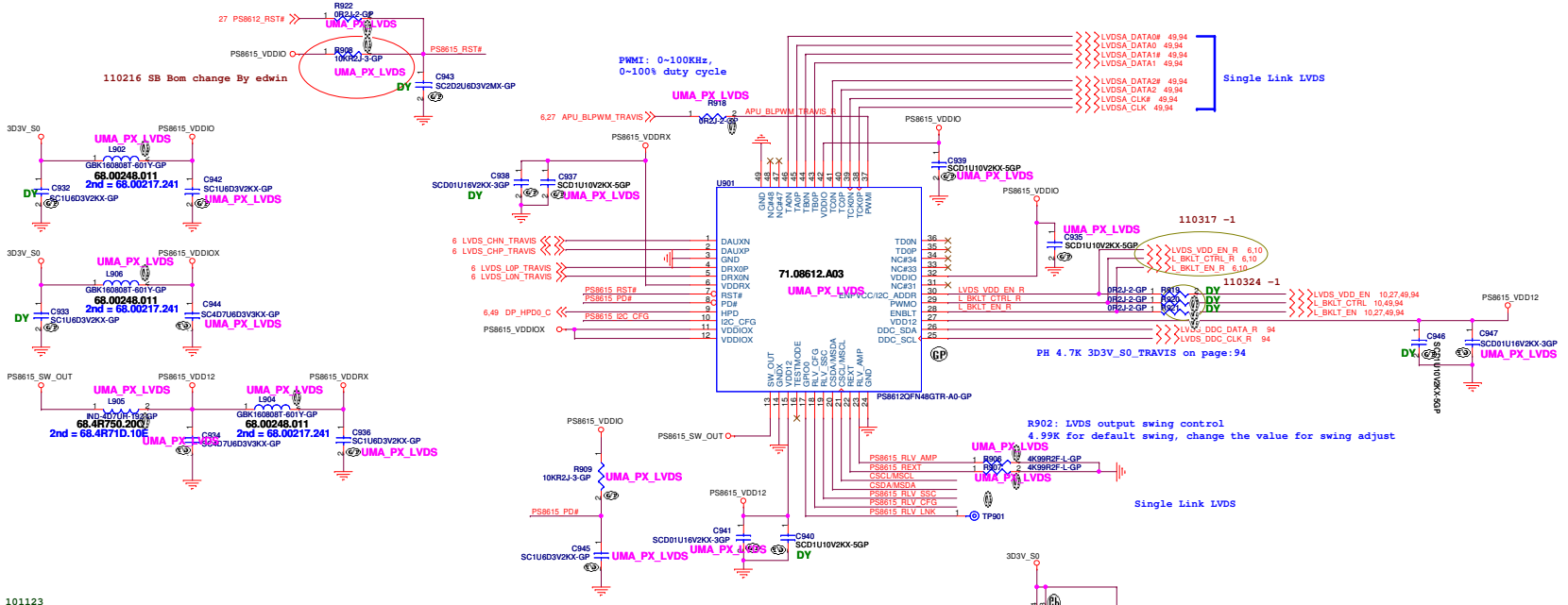

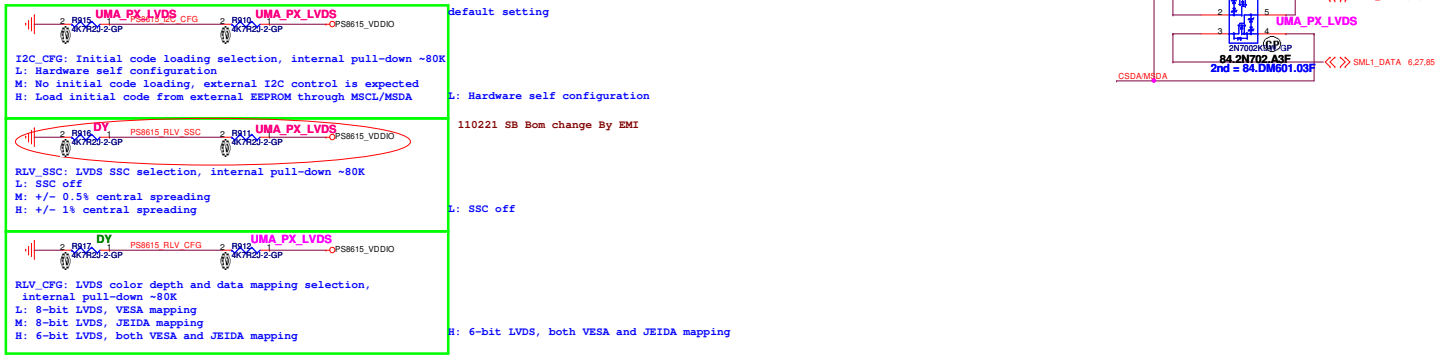

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Title: TRAVIS

Size	Document Number	Rev
A2	JE50_SB	SB

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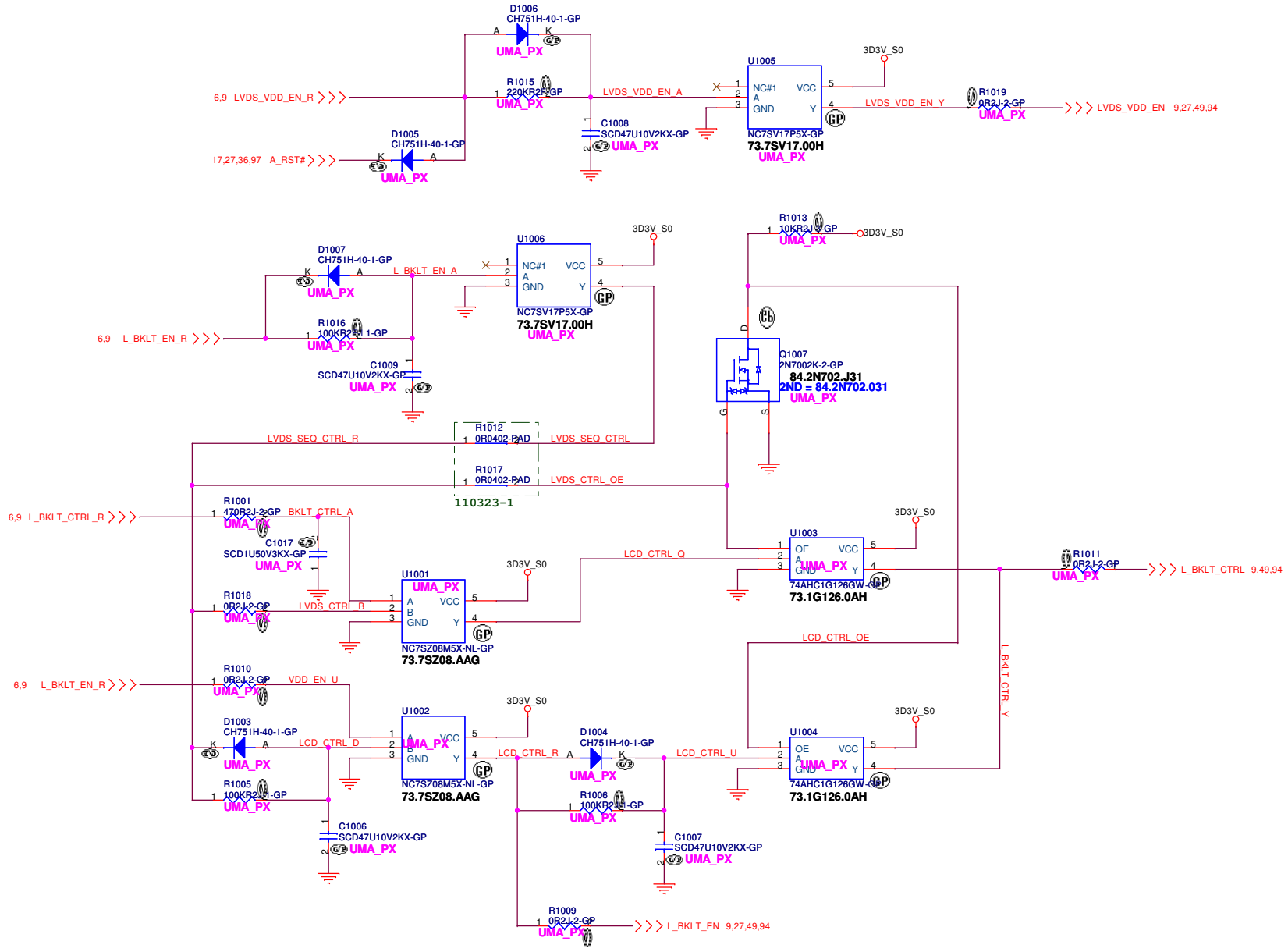

<Variant Name>

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Title: ***Reserved***

Size	Document Number	Rev
A3	JE50 SB	SB

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<Variant Name>

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Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

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<Variant Name>

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Size	Document Number	Rev
A4	JE50_SB	SB

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<Variant Name>

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Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

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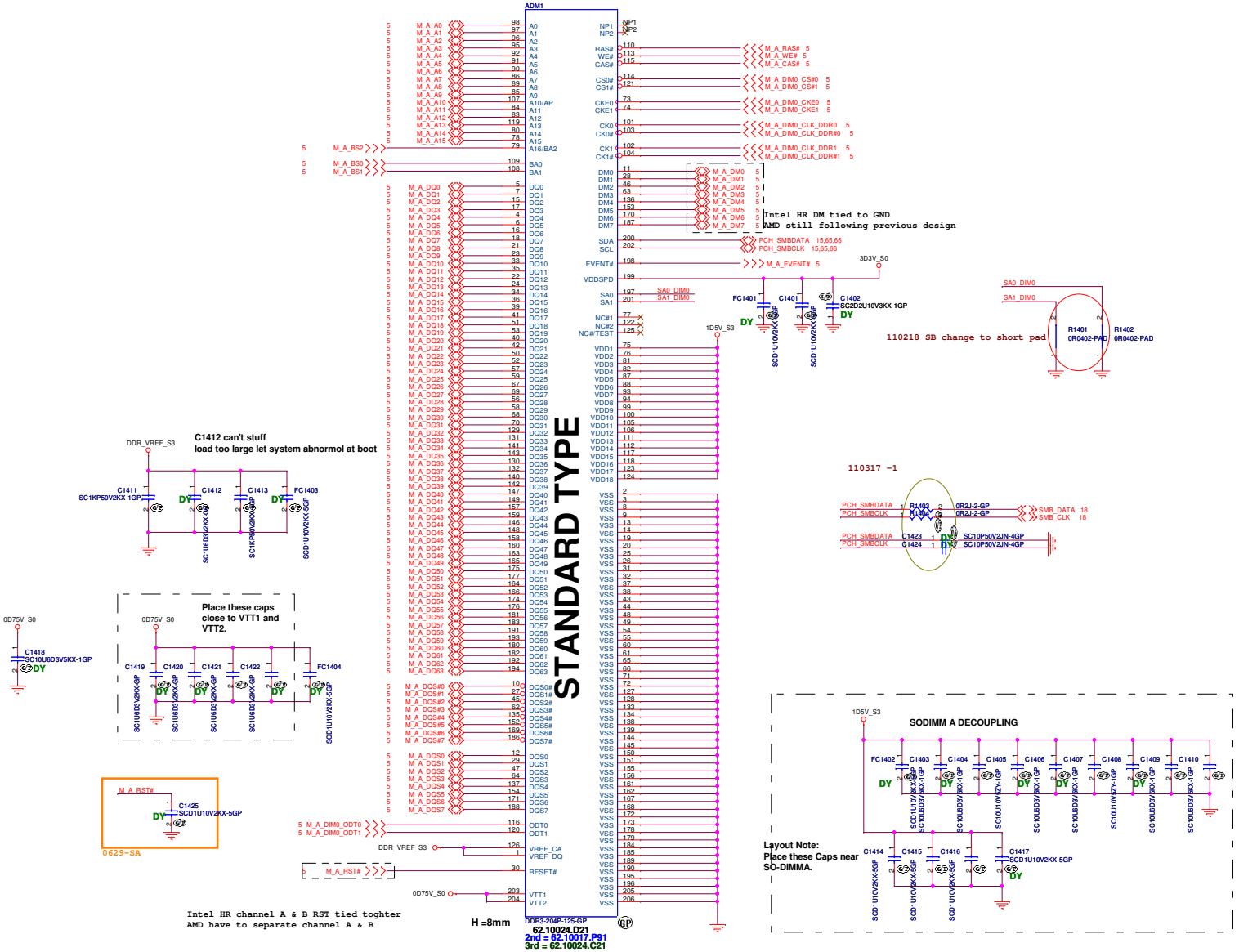

<Variant Name>

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Title: **DDR3-SODIMM1**

Size	Document Number	Rev
A2	JE50_SB	SB

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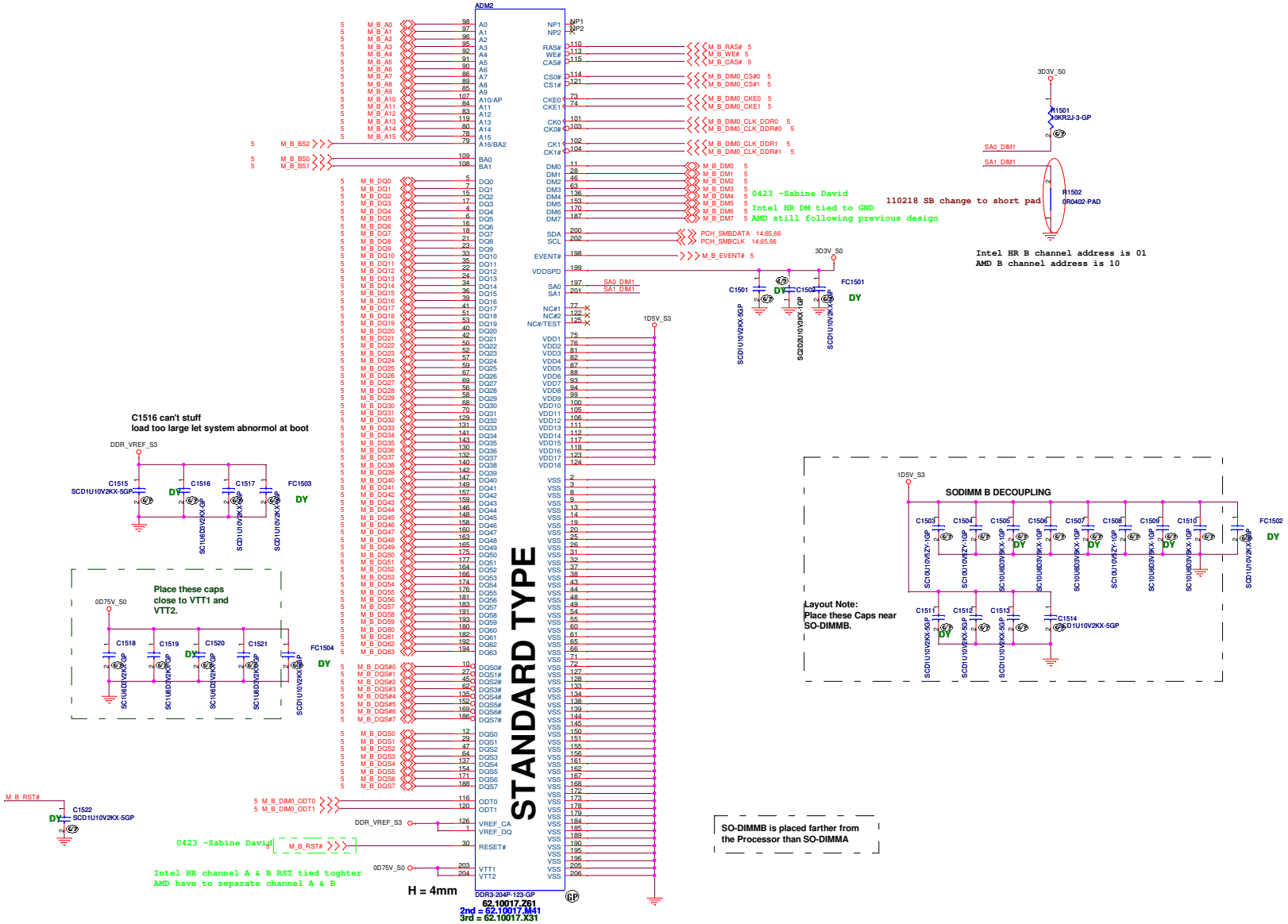

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Wistron Corporation
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Title: DDR3-SODIMM2

Size	Document Number	Rev
A2	JE50 SB	SB

Date: Friday, April 01, 2011 Sheet 15 of 102

(Blanking)

<Variant Name>

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Title

Reserved

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110307 SB change bom by siv

FCH1E

Part 5 of 5

71.HUDM2.M03

GPP CLK port	Device	CLKREQ#
0	New Card	0
1	WLAN	1
2	WWAN	2
3	LAN	3
4	X	
5	X	
6	X	
7	X	
8	X	

CL = 12pF
Freq tolertance :+/- 30ppm

110317 -1

EXT clock_Gen

For TRAVIS

1005-SA

NEW

110317 -1

Debug Strap

PX

Muxless support
PE_GPIO0 ->VGA_RESET
PE_GPIO1 ->VGA_PowerEnable

PM_CLKRUN#

checklist:No PU Res
Integrated Resistor PU10K

110218 SB change to short pad

folloiwng Intel HR netname

LDT_STP# connection is just for chipset automation purpose. It is an automatic test for AMD validation team only

-Sabin David for SW Jin define

110301 SB bom change

CL = 7pF
Freq tolertance :+/- 20 ppm

<Variant Name>

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Title: HUDSON-M2(1/6)

Size: Custom | Document Number: JE50_SB | Rev: SB

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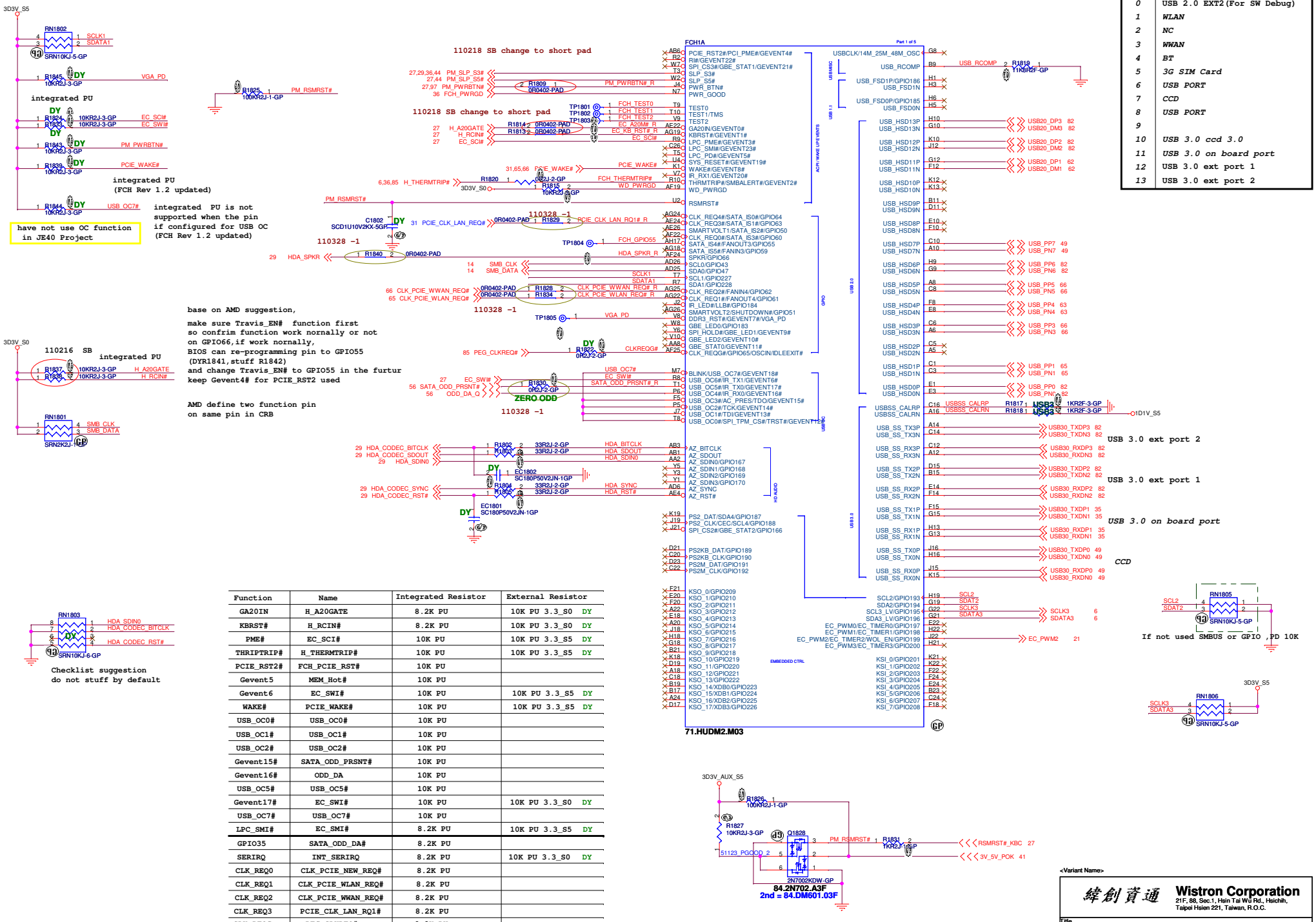
USB
Pair | Device
0 | USB 2.0 EXT2(For SW Debug)
1 | WLAN
2 | NC
3 | WWAN
4 | BT
5 | 3G SIM Card
6 | USB PORT
7 | CCD
8 | USB PORT
9 |
10 | USB 3.0 ccd 3.0
11 | USB 3.0 on board port
12 | USB 3.0 ext port 1
13 | USB 3.0 ext port 2
integrated PU
integrated PU (FCH Rev 1.2 updated)
integrated PU is not supported when the pin if configured for USB OC (FCH Rev 1.2 updated)
have not use OC function in JE40 Project
110218 SB change to short pad
110218 SB change to short pad
110328 -1
110328 -1
110328 -1
110328 -1
110216 SB
integrated PU
base on AMD suggestion,
make sure Travis_EN# function first so confrim function work normally or not on GPIO66,if work normally, BIOS can re-programming pin to GPIO55 (DYR1841,stuff R1842) and change Travis_EN# to GPIO55 in the furtur keep Gevent4# for PCIE_RST2 used
AMD define two function pin on same pin in CRB
ZERO ODD
FCH1A
Part 1 of 5
USB 3.0 ext port 2
USB 3.0 ext port 1
USB 3.0 on board port
CCD
If not used SMBUS or GPIO ,PD 10K
Checklist suggestion do not stuff by default
71.HUDM2.M03
84.2N702.A3F
2nd = 84.DM601.03F
Function | Name | Integrated Resistor | External Resistor
GA20IN | H_A20GATE | 8.2K PU | 10K PU 3.3_S0 DY
KBRST# | H_RCIN# | 8.2K PU | 10K PU 3.3_S0 DY
PME# | EC_SCI# | 10K PU | 10K PU 3.3_S5 DY
THRIPTRIP# | H_THERMTRIP# | 10K PU | 10K PU 3.3_S5 DY
PCIE_RST2# | FCH_PCIE_RST# | 10K PU |
Gevent5 | MEM_Hot# | 10K PU |
Gevent6 | EC_SWI# | 10K PU | 10K PU 3.3_S5 DY
WAKE# | PCIE_WAKE# | 10K PU | 10K PU 3.3_S5 DY
USB_OC0# | USB_OC0# | 10K PU |
USB_OC1# | USB_OC1# | 10K PU |
USB_OC2# | USB_OC2# | 10K PU |
Gevent15# | SATA_ODD_PRSNT# | 10K PU |
Gevent16# | ODD_DA | 10K PU |
USB_OC5# | USB_OC5# | 10K PU |
Gevent17# | EC_SWI# | 10K PU | 10K PU 3.3_S0 DY
USB_OC7# | USB_OC7# | 10K PU |
LPC_SMI# | EC_SMI# | 8.2K PU | 10K PU 3.3_S5 DY
GPIO35 | SATA_ODD_DA# | 8.2K PU |
SERIRQ | INT_SERIRQ | 8.2K PU | 10K PU 3.3_S0 DY
CLK_REQ0 | CLK_PCIE_NEW_REQ# | 8.2K PU |
CLK_REQ1 | CLK_PCIE_WLAN_REQ# | 8.2K PU |
CLK_REQ2 | CLK_PCIE_WWAN_REQ# | 8.2K PU |
CLK_REQ3 | PCIE_CLK_LAN_RQ1# | 8.2K PU |
CLK_REQG | PEG_CLKREQ# | 8.2K PU |
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
HUDSON-M2(2/6)
Size Custom
Document Number JE50 SB
Rev SB
Date: Friday, April 01, 2011
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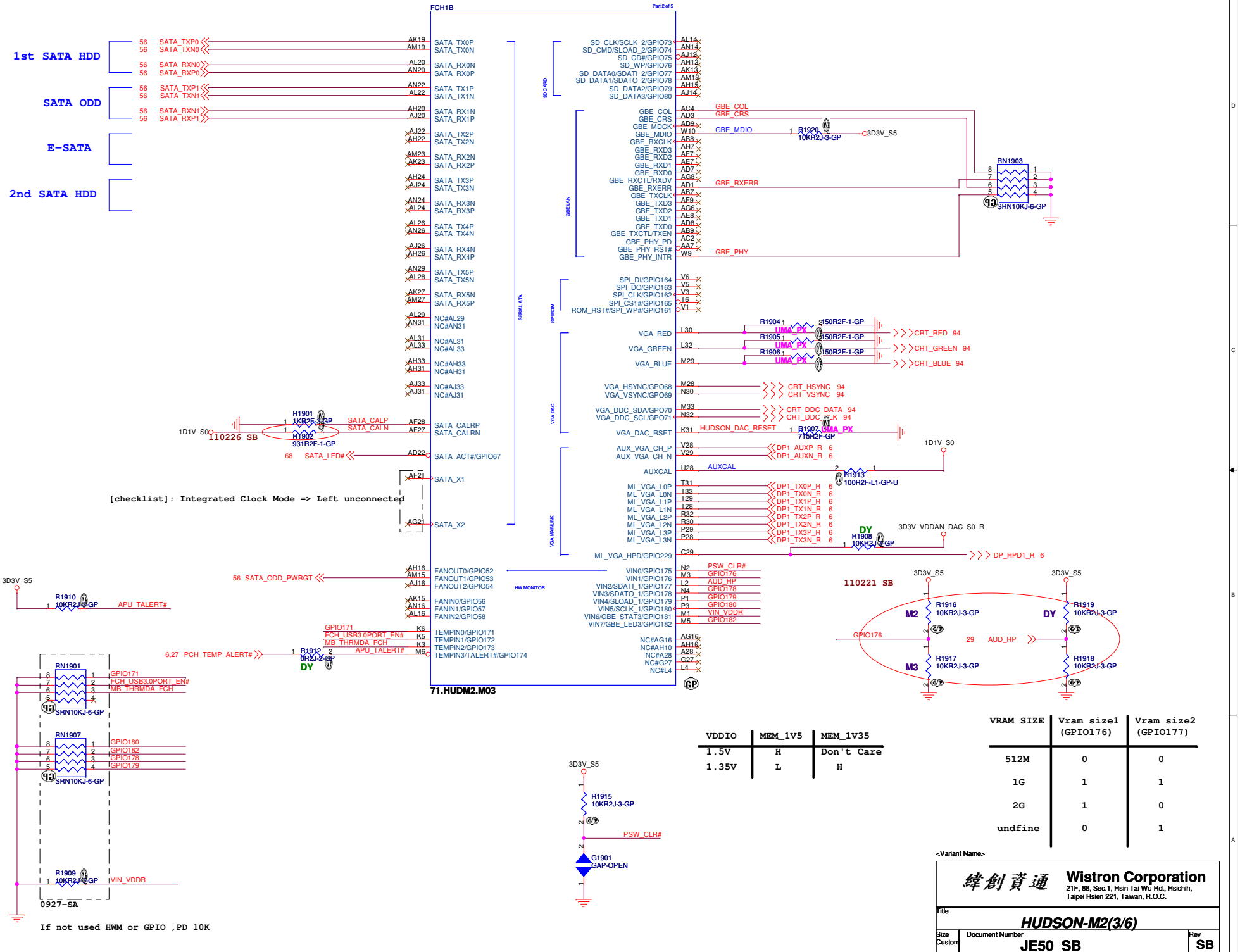

VDDIO	MEM_1V5	MEM_1V35
1.5V	H	Don't Care
1.35V	L	H

VRAM SIZE	Vram size1 (GPIO176)	Vram size2 (GPIO177)
512M	0	0
1G	1	1
2G	1	0
undfine	0	1

<Variant Name>

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Title: HUDSON-M2(3/6)

Size: Custom | Document Number: JE50_SB | Rev: SB

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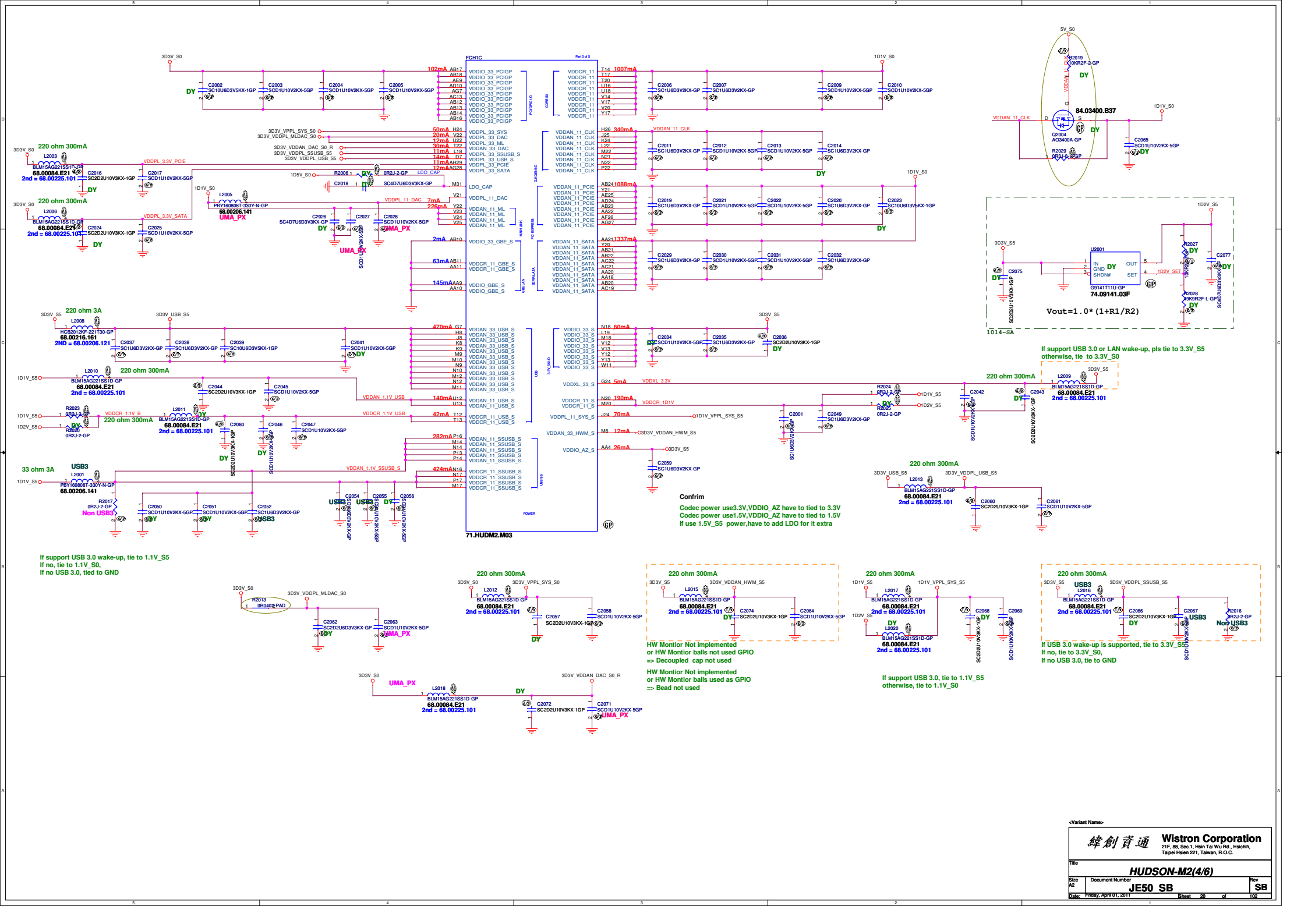

<Variant Name>

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Title: HUDSON-M2(4/6)

Size	Document Number	Rev
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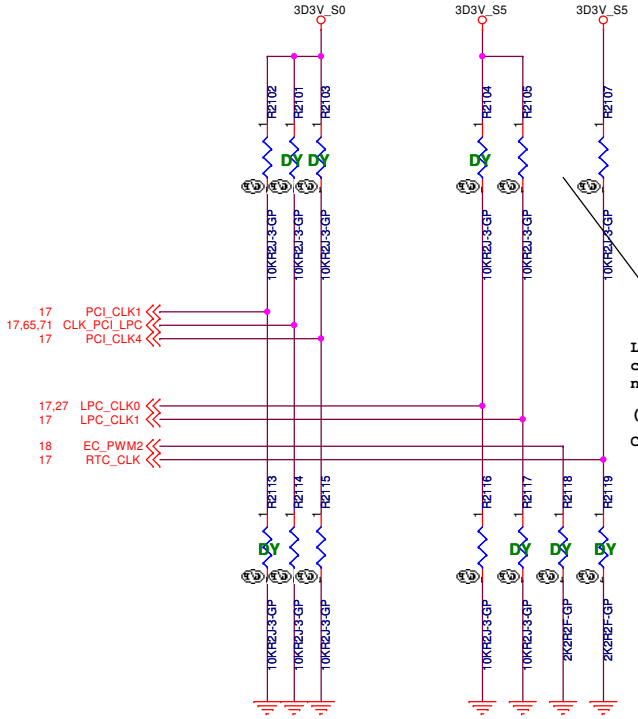
SSID = S.B

REQUIRED STRAPS

CRB:PU 3.3V_AUX_S5

checklist:PU 3.3V_S5

no support S5 PLUS funciton,PU 3.3V_S5



LPC ROM implemented
checklistsuggestion:
no PU or PD required

(integrated PU 10K)

CRB: do not stuff PU Res

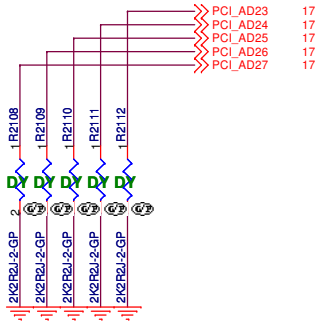
REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

Ball Name	Strap Function	Description
EC_PWM2	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V_S5. External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

<Variant Name>

緯創資通 Wistron Corporation
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Title: HUDSON-M2(5/6)

Size: A3 | Document Number: JE50_SB | Rev: SB

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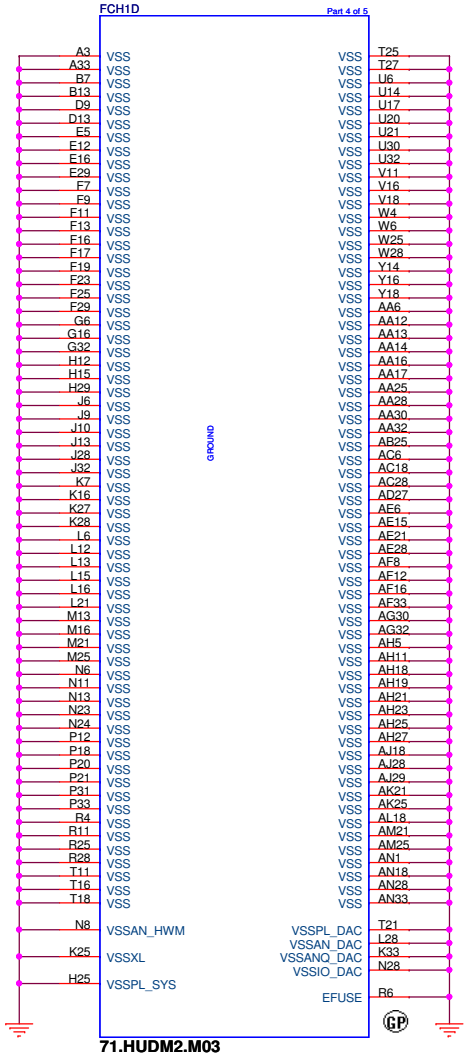

71.HUDM2.M03

<Variant Name>

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Title: ***HUDSON-M2(6/6)***

Size	Document Number	Rev
A3	**JE50_SB**	**SB**

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<Variant Name>

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Title
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Size	Document Number	Rev
A4	JE50_SB	SB

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<Variant Name>

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Size	Document Number	Rev
A4	JE50_SB	SB

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Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 25 of 102

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<Variant Name>

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Title

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Size	Document Number	Rev
A4	JE50_SB	SB

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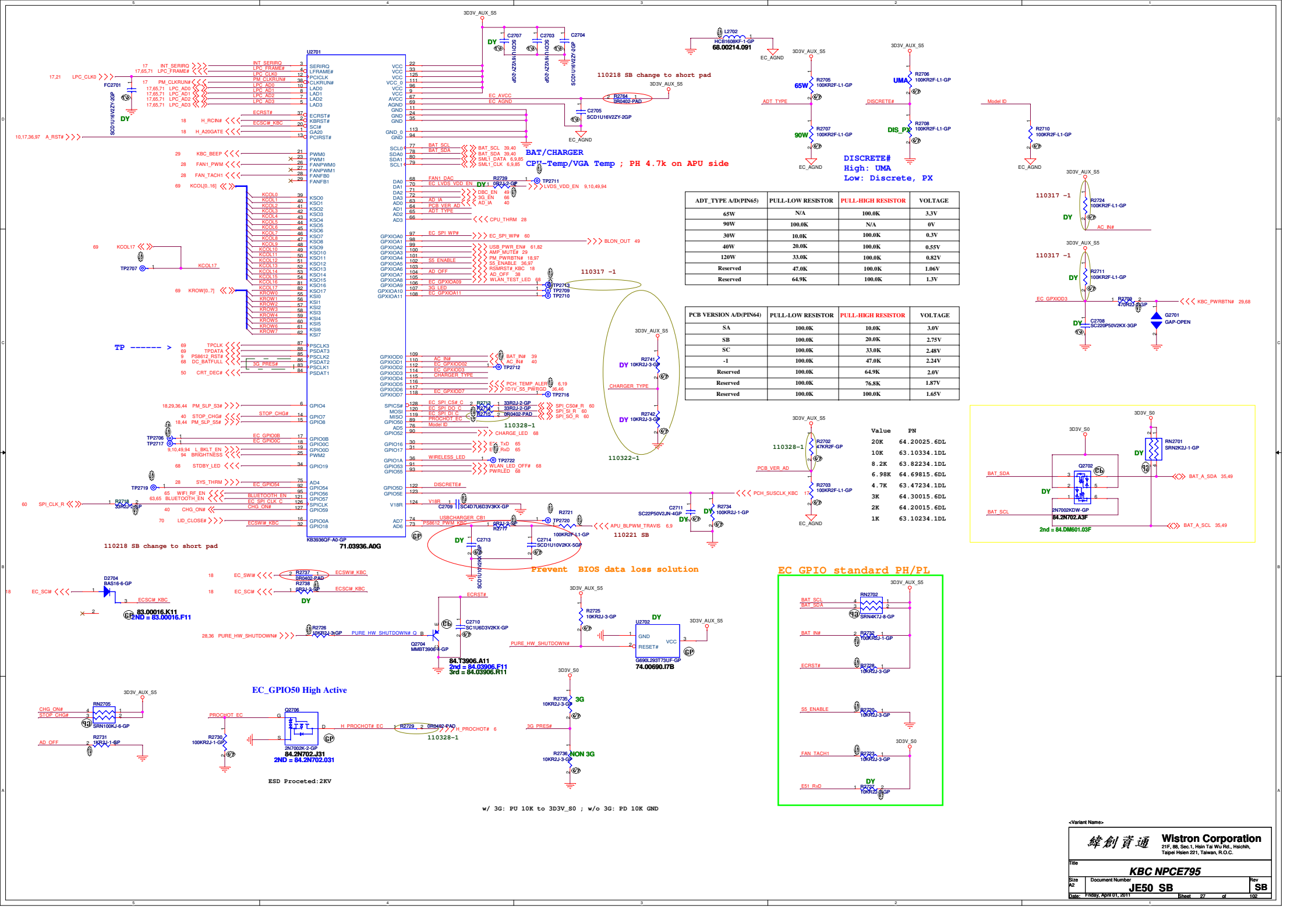


ADT_TYPE A/D(PIN65)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

PCB VERSION A/D(PIN64)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

Value	PN
20K	64.20025.6DL
10K	63.10334.1DL
8.2K	63.82234.1DL
6.98K	64.69815.6DL
4.7K	63.47234.1DL
3K	64.30015.6DL
2K	64.20015.6DL
1K	63.10234.1DL

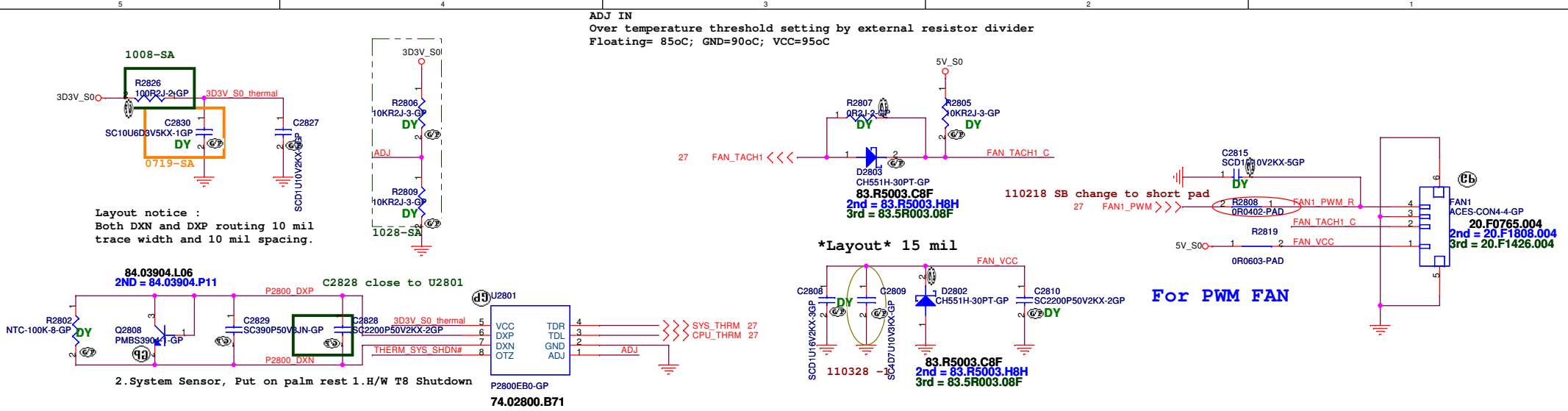
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

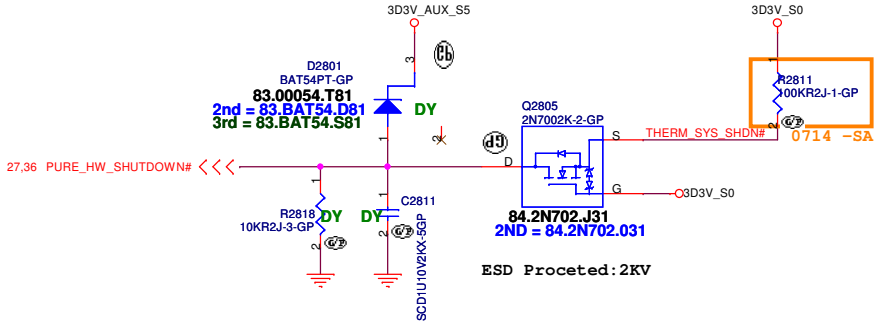
Title: KBC NPCE795

Size	Document Number	Rev
A2	JE50 SB	SB

Date: Friday, April 01, 2011 Sheet 27 of 102



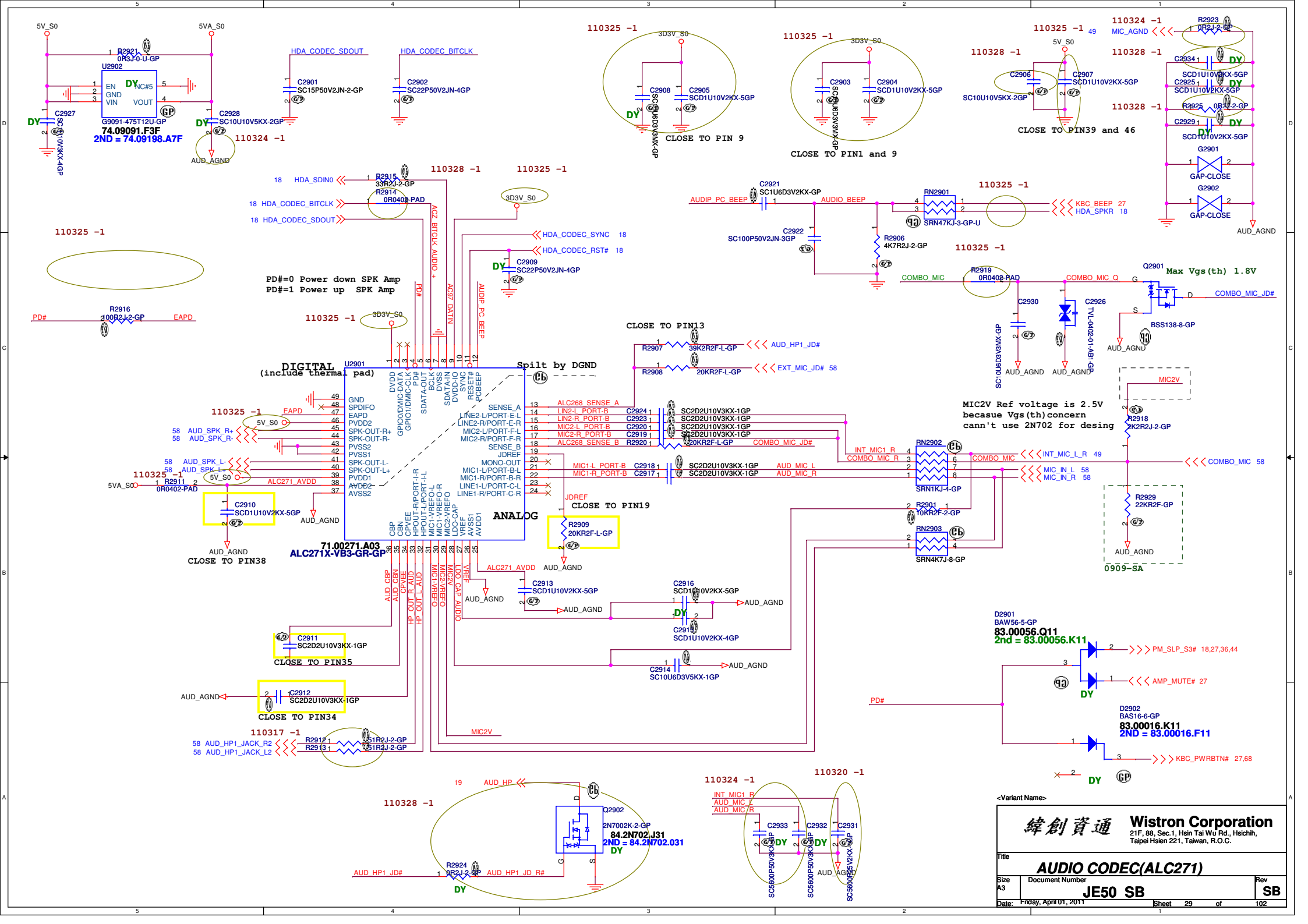
VGA Thermal sensor P2800



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Thermal P2800*	
Size A3	Document Number JE50_SB	Rev SB
Date: Friday, April 01, 2011	Sheet 28 of 102	


DIGITAL
(include thermal pad)
ANALOG
Spilt by DGND
71.00271.A03
ALC271X-VB3-GR-GP
74.09091.F3F
2ND = 74.09198.A7F
G9091-475T12U-GP
PD#=0 Power down SPK Amp
PD#=1 Power up SPK Amp
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN19
CLOSE TO PIN13
CLOSE TO PIN9
CLOSE TO PIN1 and 9
CLOSE TO PIN39 and 46
MIC2V Ref voltage is 2.5V
becasue Vgs(th)concern
cann't use 2N702 for desing
Max Vgs(th) 1.8V
83.00056.Q11
2nd = 83.00056.K11
83.00016.K11
2ND = 83.00016.F11
84.2N702.J31
2ND = 84.2N702.031
0909-SA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC(ALC271)
JE50 SB
Friday, April 01, 2011
Sheet 29 of 102

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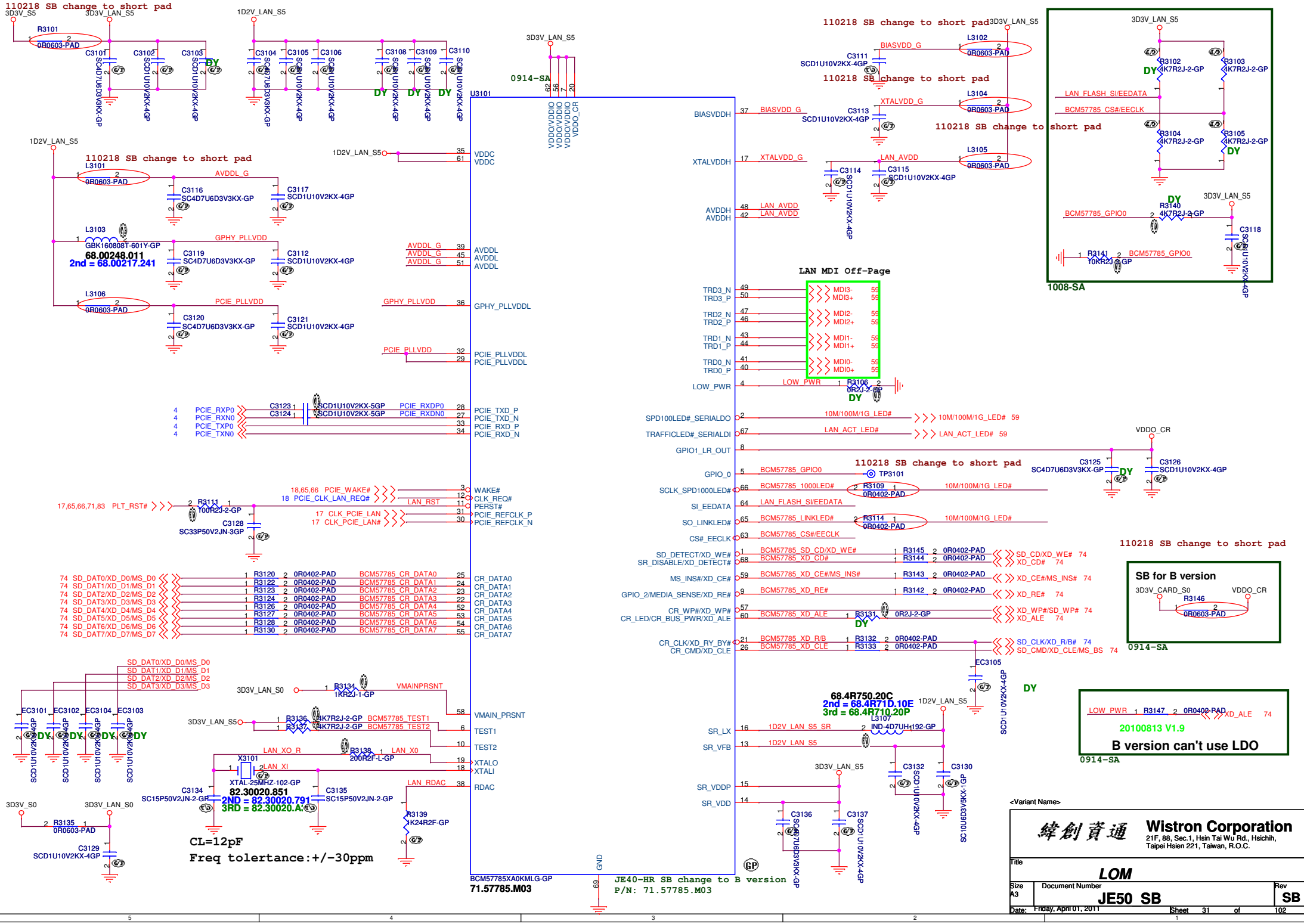
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMP

Size: A4 | Document Number: JE50_SB | Rev: SB

Date: Friday, April 01, 2011 | Sheet 30 of 102


110218 SB change to short pad
3D3V_S5
3D3V_LAN_S5
1D2V_LAN_S5
R3101
0R0603-PAD
C3101
SCD47U6D3V3KX-GP
C3102
SCD1U10V2KX-4GP
C3103
DY
C3104
C3105
C3106
C3108
C3109
C3110
0914-SA
U3101
VDDO/VDDIO
VDDO/VDDIO
VDDO/VDDIO
VDDO_CR
L3101
AVDDL_G
C3116
SC4D7U6D3V3KX-GP
C3117
SCD1U10V2KX-4GP
L3103
GBK160808T-601Y-GP
68.00248.011
2nd = 68.00217.241
GPHY_PLLVDD
C3119
C3112
L3106
PCIE_PLLVDD
C3120
C3121
VDDC
AVDDL
GPHY_PLLVDDL
PCIE_PLLVDDL
PCIE_RXP0
PCIE_RXN0
PCIE_TXP0
PCIE_TXN0
C3123
C3124
SCD1U10V2KX-5GP
PCIE_RXDP0
PCIE_RXDN0
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
18,65,66 PCIE_WAKE#
18 PCIE_CLK_LAN_REQ#
LAN_RST
17,65,66,71,83 PLT_RST#
R3111
100R2J-2-GP
C3128
SC33P50V2JN-3GP
WAKE#
CLK_REQ#
PERST#
17 CLK_PCIE_LAN
17 CLK_PCIE_LAN#
PCIE_REFCLK_P
PCIE_REFCLK_N
74 SD_DAT0/XD_D0/MS_D0
74 SD_DAT1/XD_D1/MS_D1
74 SD_DAT2/XD_D2/MS_D2
74 SD_DAT3/XD_D3/MS_D3
74 SD_DAT4/XD_D4/MS_D4
74 SD_DAT5/XD_D5/MS_D5
74 SD_DAT6/XD_D6/MS_D6
74 SD_DAT7/XD_D7/MS_D7
R3120
R3122
R3123
R3124
R3126
R3127
R3128
R3130
0R0402-PAD
BCM57785_CR_DATA0
BCM57785_CR_DATA1
BCM57785_CR_DATA2
BCM57785_CR_DATA3
BCM57785_CR_DATA4
BCM57785_CR_DATA5
BCM57785_CR_DATA6
BCM57785_CR_DATA7
CR_DATA0
CR_DATA1
CR_DATA2
CR_DATA3
CR_DATA4
CR_DATA5
CR_DATA6
CR_DATA7
SD_DAT0/XD_D0/MS_D0
SD_DAT1/XD_D1/MS_D1
SD_DAT2/XD_D2/MS_D2
SD_DAT3/XD_D3/MS_D3
EC3101
EC3102
EC3104
EC3103
3D3V_LAN_S0
R3134
1KR2J-1-GP
VMAINPRSNT
VMAIN_PRSNT
R3136
R3137
4K7R2J-2-GP
BCM57785_TEST1
BCM57785_TEST2
TEST1
TEST2
LAN_XO_R
R3138
200R2F-L-GP
LAN_XO
X3101
XTAL-25MHZ-102-GP
LAN_XI
XTALO
XTALI
82.30020.851
2ND = 82.30020.791
3RD = 82.30020.A
C3134
SC15P50V2JN-2GP
C3135
SC15P50V2JN-2-GP
LAN_RDAC
R3139
K24R2F-GP
RDAC
CL=12pF
Freq tolertance:+/-30ppm
3D3V_S0
R3135
0R0603-PAD
C3129
SCD1U10V2KX-4GP
BCM57785XA0KMLG-GP
71.57785.M03
GND
JE40-HR SB change to B version
P/N: 71.57785.M03
BIASVDDH
BIASVDD_G
XTALVDDH
XTALVDD_G
AVDDH
LAN_AVDDH
LAN_AVDD
C3111
C3113
C3114
C3115
L3102
L3104
L3105
LAN MDI Off-Page
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
LOW_PWR
R3106
0R2J-2-GP
SPD100LED#_SERIALDO
TRAFFICLED#_SERIALDI
GPIO1_LR_OUT
10M/100M/1G_LED#
LAN_ACT_LED#
GPIO_0
SCLK_SPD1000LED#
SI_EEDATA
SO_LINKLED#
CS#_EECLK
BCM57785_GPIO0
BCM57785_1000LED#
BCM57785_EEDATA
BCM57785_LINKLED#
BCM57785_CS#/EECLK
TP3101
R3109
R3114
SD_DETECT/XD_WE#
SR_DISABLE/XD_DETECT#
MS_INS#/XD_CE#
GPIO_2/MEDIA_SENSE/XD_RE#
CR_WP#/XD_WP#
CR_LED/CR_BUS_PWR/XD_ALE
CR_CLK/XD_RY_BY#
CR_CMD/XD_CLE
BCM57785_SD_CD/XD_WE#
BCM57785_XD_CD#
BCM57785_XD_CE#/MS_INS#
BCM57785_XD_RE#
BCM57785_XD_ALE
BCM57785_XD_R/B
BCM57785_XD_CLE
R3145
R3144
R3143
R3142
R3131
R3132
R3133
0R2J-2-GP
SD_CD/XD_WE#
XD_CD#
XD_CE#/MS_INS#
XD_RE#
XD_WP#/SD_WP#
XD_ALE
SD_CLK/XD_R/B#
SD_CMD/XD_CLE/MS_BS
C3125
SC4D7U6D3V3KX-GP
C3126
SCD1U10V2KX-4GP
VDDO_CR
SR_LX
SR_VFB
SR_VDDP
SR_VDD
1D2V_LAN_S5_SR
L3107
IND-4D7UH-192-GP
68.4R750.20C
2nd = 68.4R710.10E
3rd = 68.4R710.20P
EC3105
SCD1U10V2KX-4GP
C3132
C3130
SC10U6D3V5KX-GP
C3136
SCD47U6D3V3KX-GP
C3137
SCD1U10V2KX-4GP
1008-SA
R3102
R3103
R3104
R3105
4K7R2J-2-GP
LAN_FLASH_SI/EEDATA
BCM57785_CS#/EECLK
R3140
R3141
10KR2J-3-GP
C3118
SCD1U10V2KX-4GP
SB for B version
3D3V_CARD_S0
R3146
0R0603-PAD
0914-SA
LOW_PWR
R3147
20100813 V1.9
B version can't use LDO
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LOM
Size
A3
Document Number
JE50 SB
Rev
SB
Date: Friday, April 01, 2011
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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RTS5138

Size	Document Number	Rev
A4	**JE50_SB**	**SB**

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 33 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

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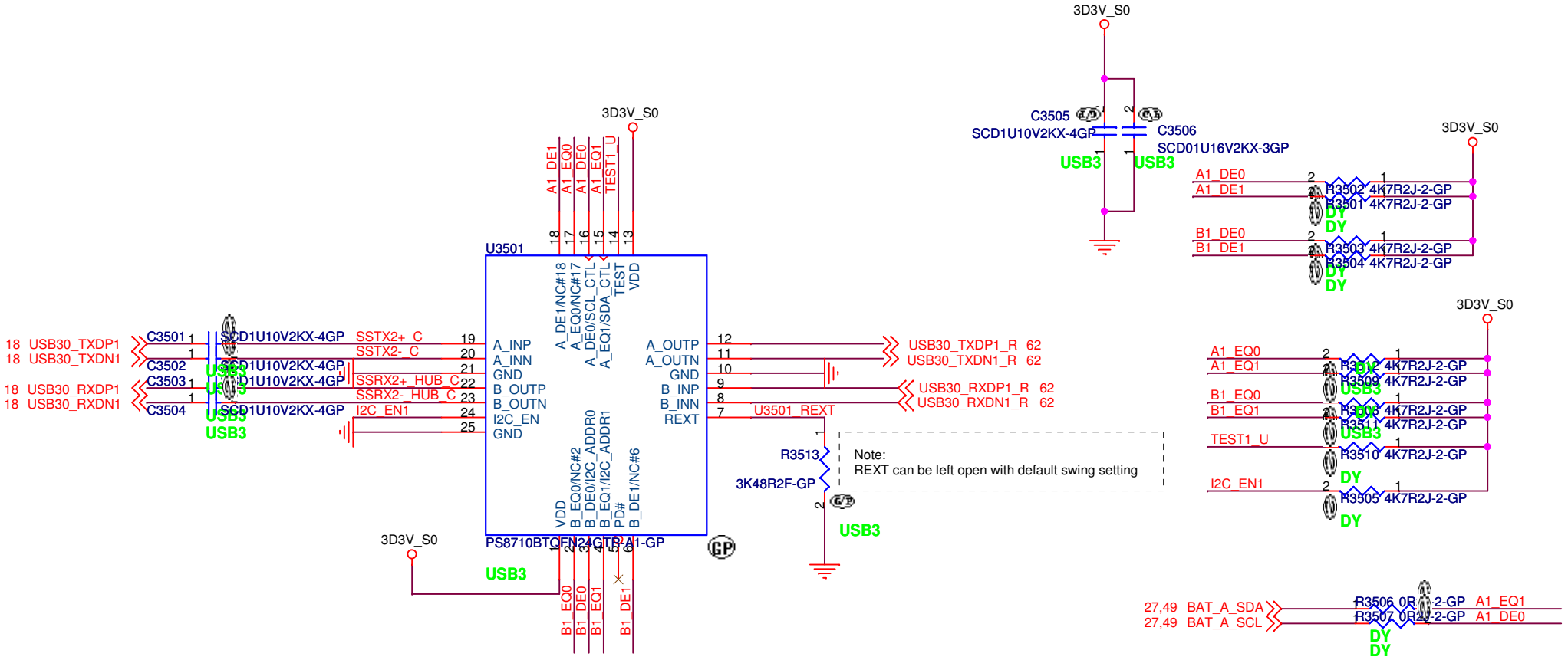

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	JE50_SB	SB

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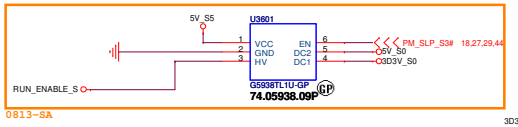
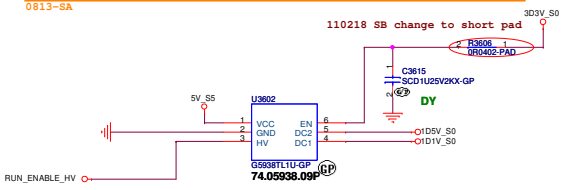
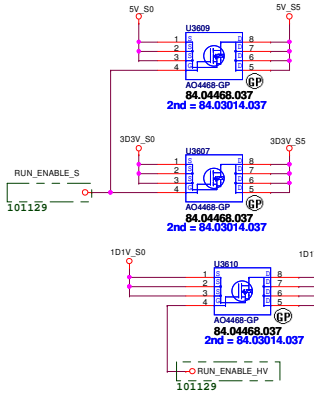
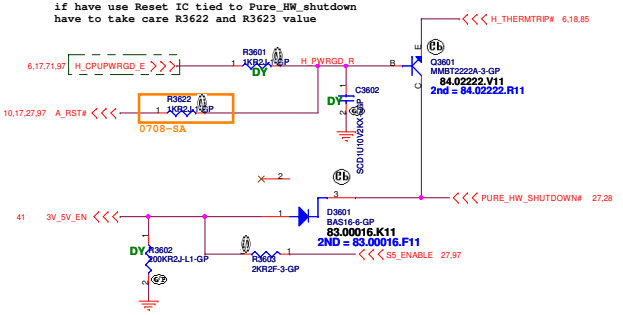
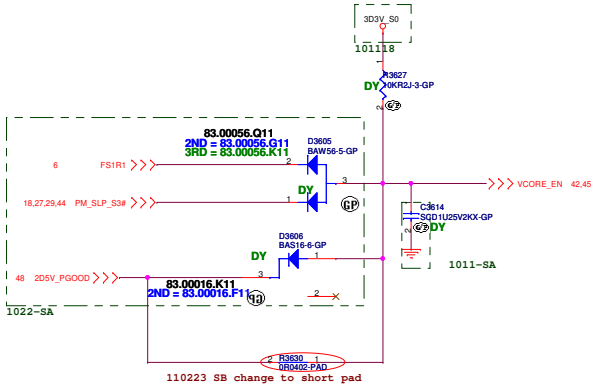


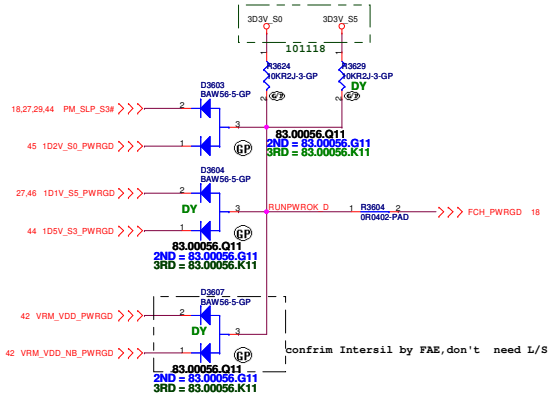






Power Sequence





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Title	Power On Logic	
Size: Custom	Document Number: JE50 SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 36 of 102	

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

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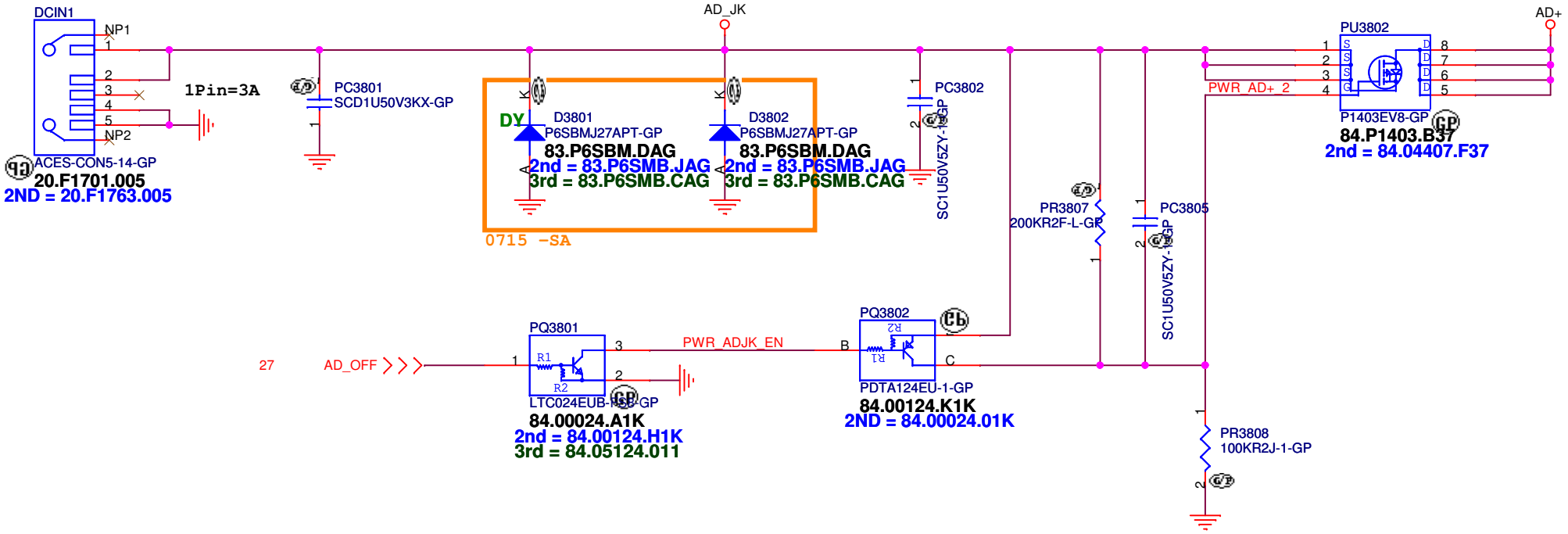
Adaptor in to generate DCBATOUT



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN_JACK*		
Size: A4	Document Number: JE50_SB	Rev: SB
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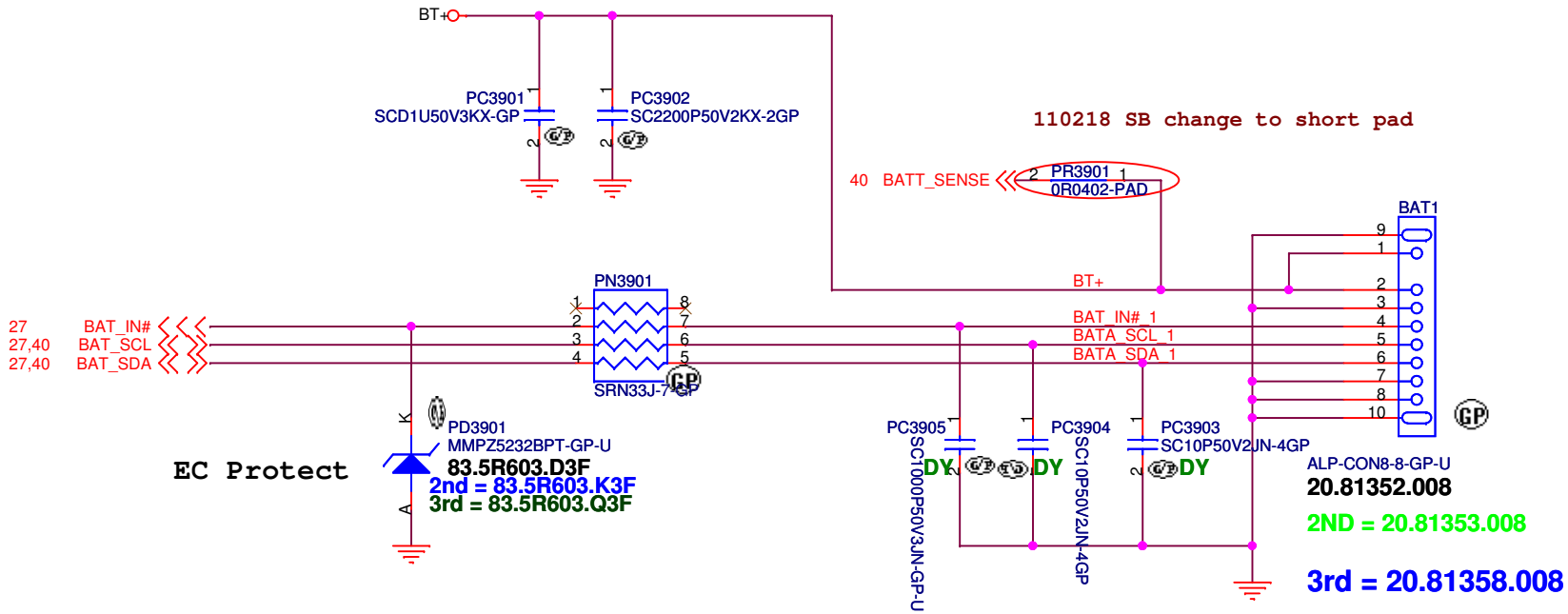
BATTERY CONNECTOR



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT_CONN	
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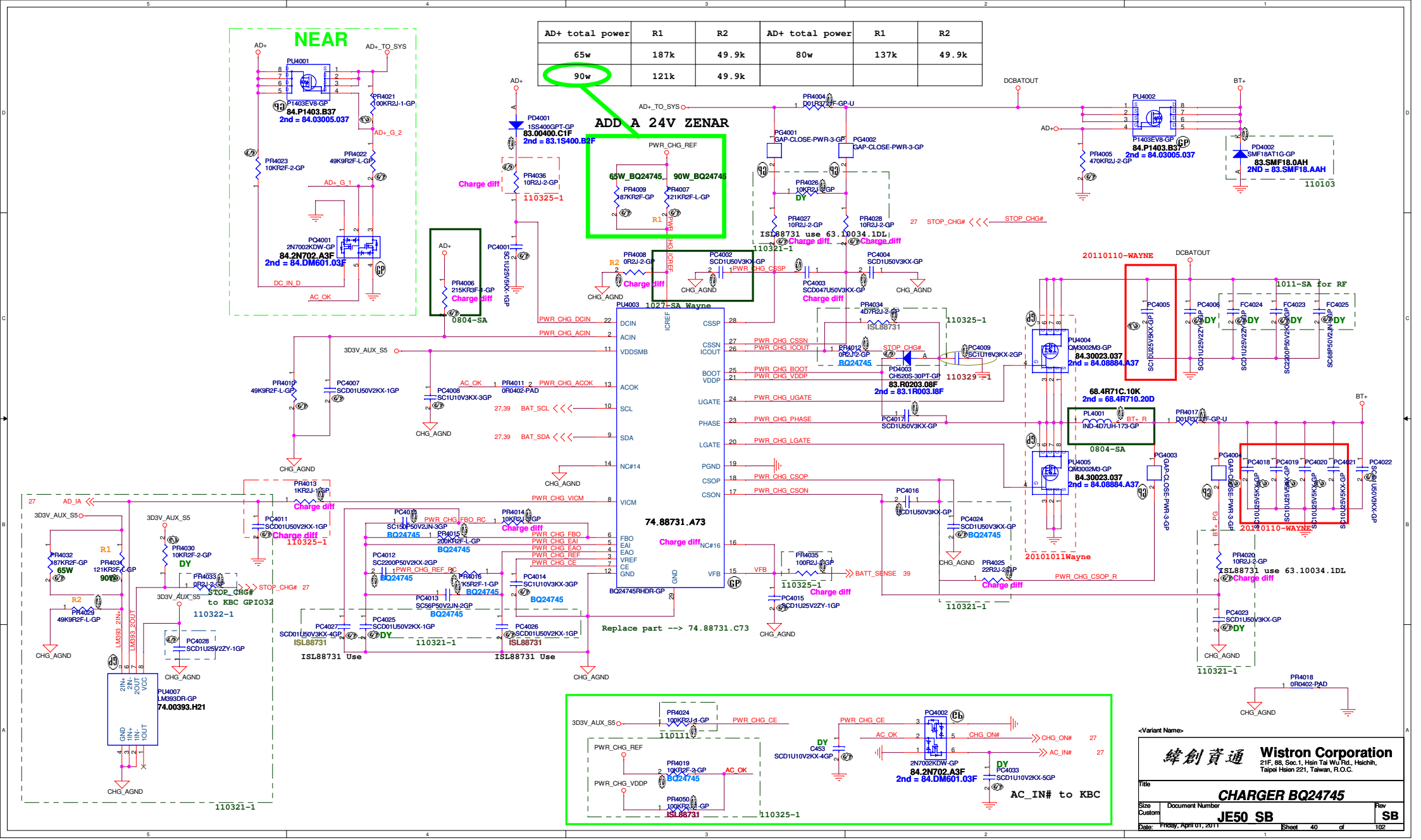
AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

ADD A 24V ZENAR

NEAR



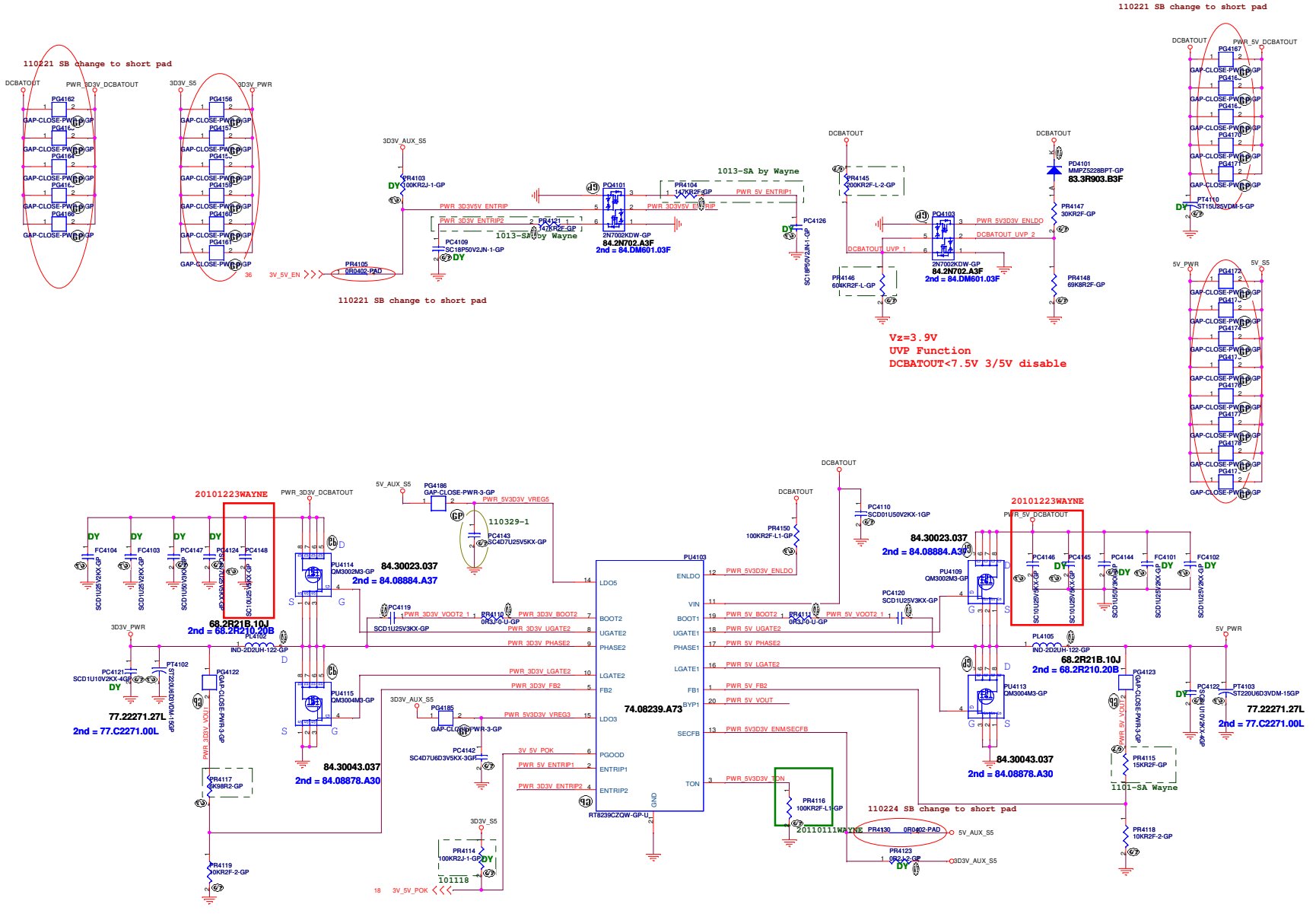
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size: Custom | Document Number: JE50_SB | Rev: SB

Date: Friday, April 01, 2011 | Sheet 40 of 102



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8239

Size	Document Number	Rev
A2	JE50 SB	SB

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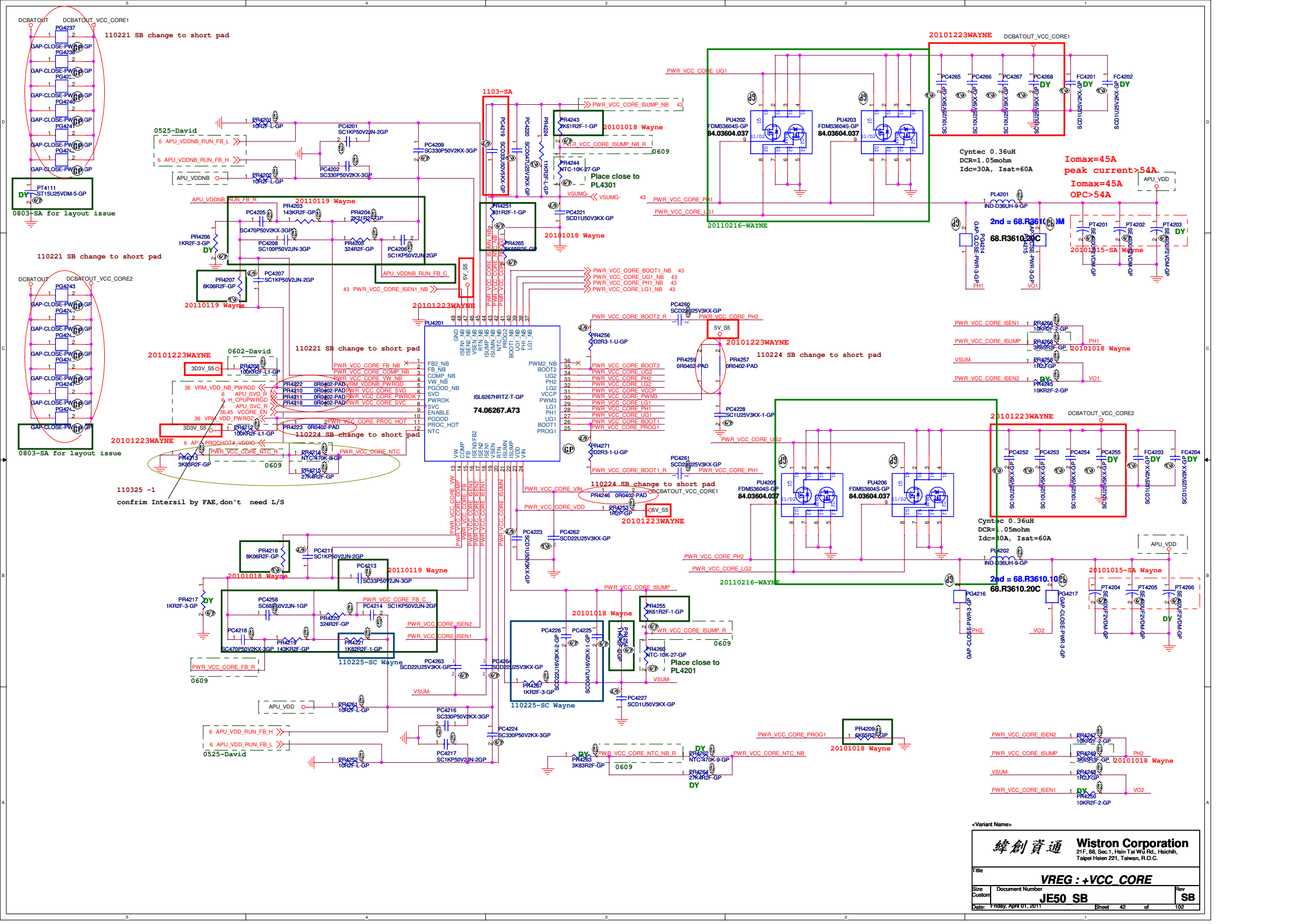

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +VCC_CORE

Size: Custom | Document Number: JE50_SB | Rev: SB

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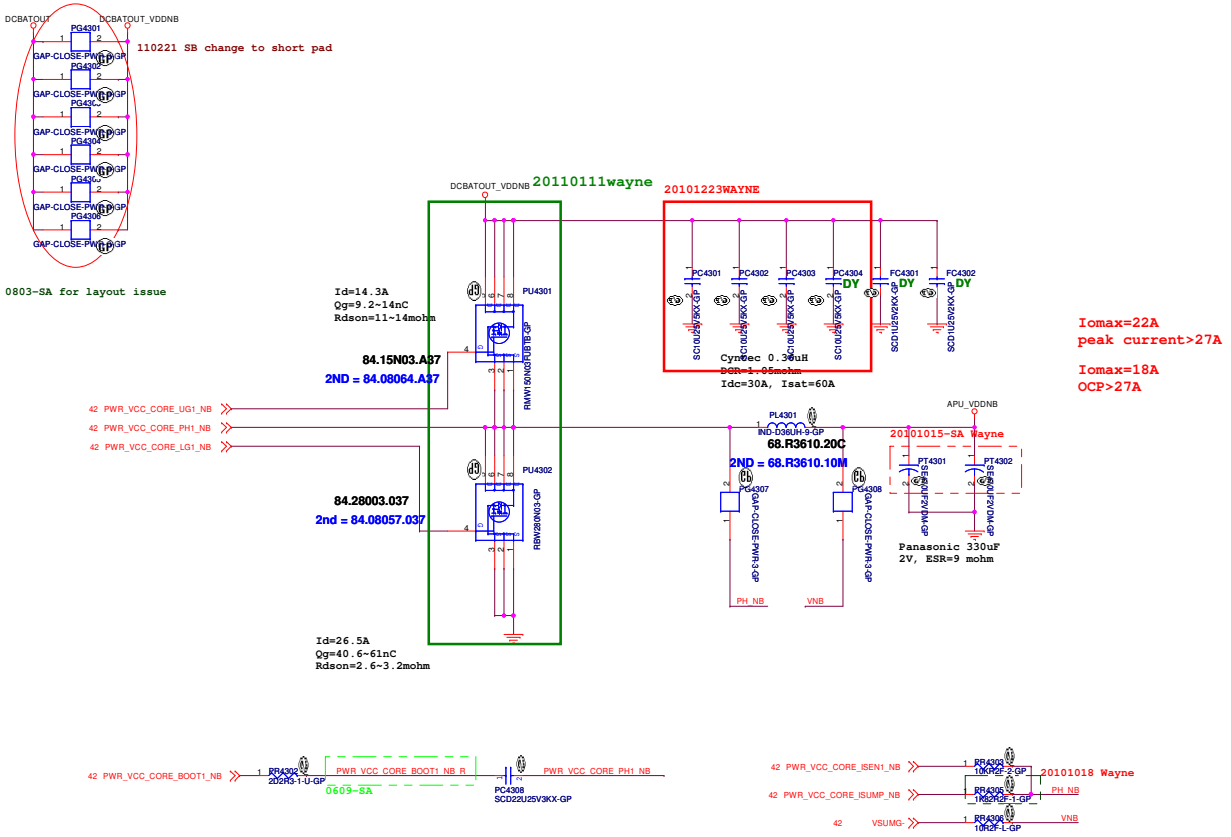

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +VCC_NB

Size: A2 | Document Number: JE50_SB | Rev: SB

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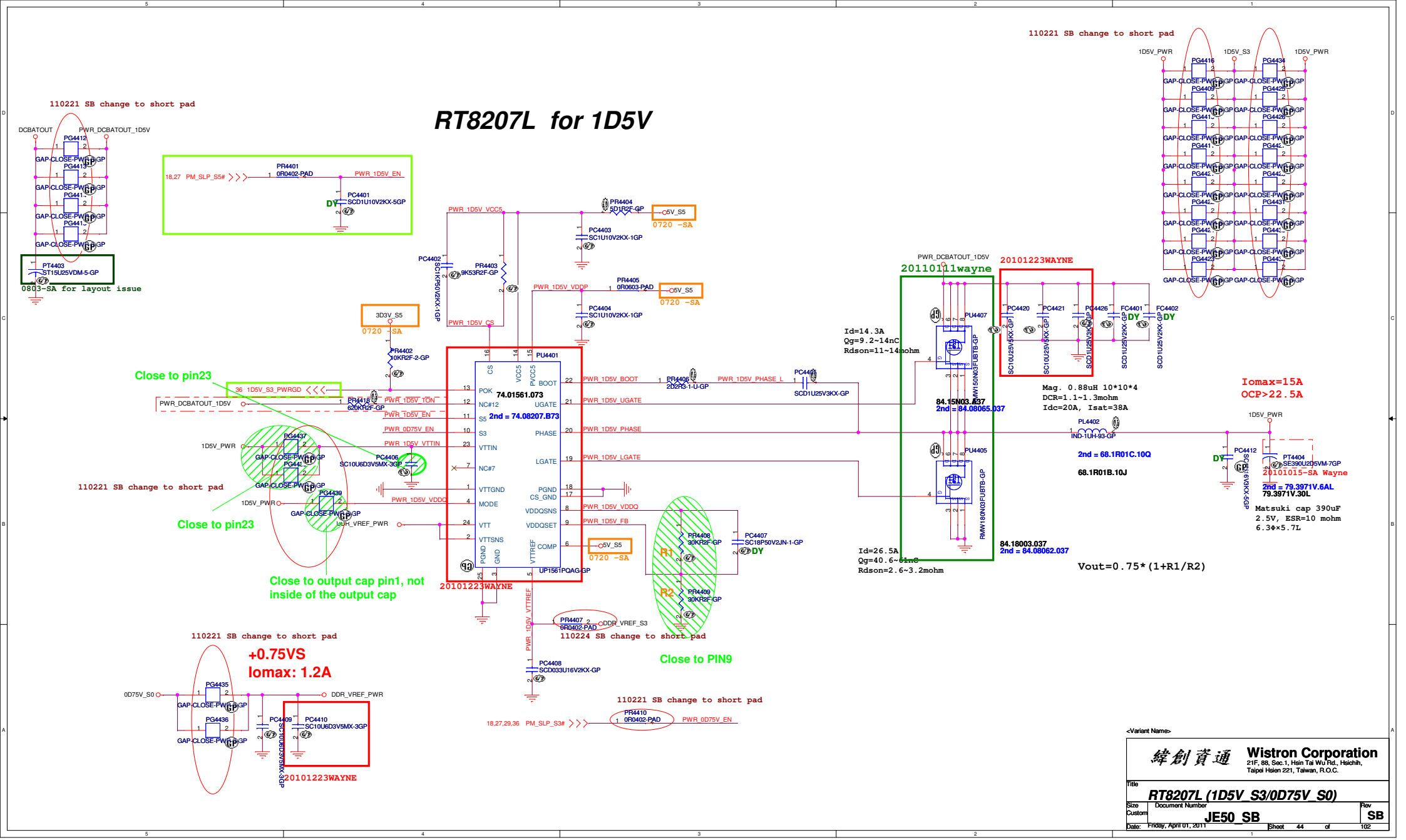
RT8207L for 1D5V



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8207L (1D5V_S3/0D75V_S0)		
Size: Custom	Document Number: JE50_SB	Rev: SB
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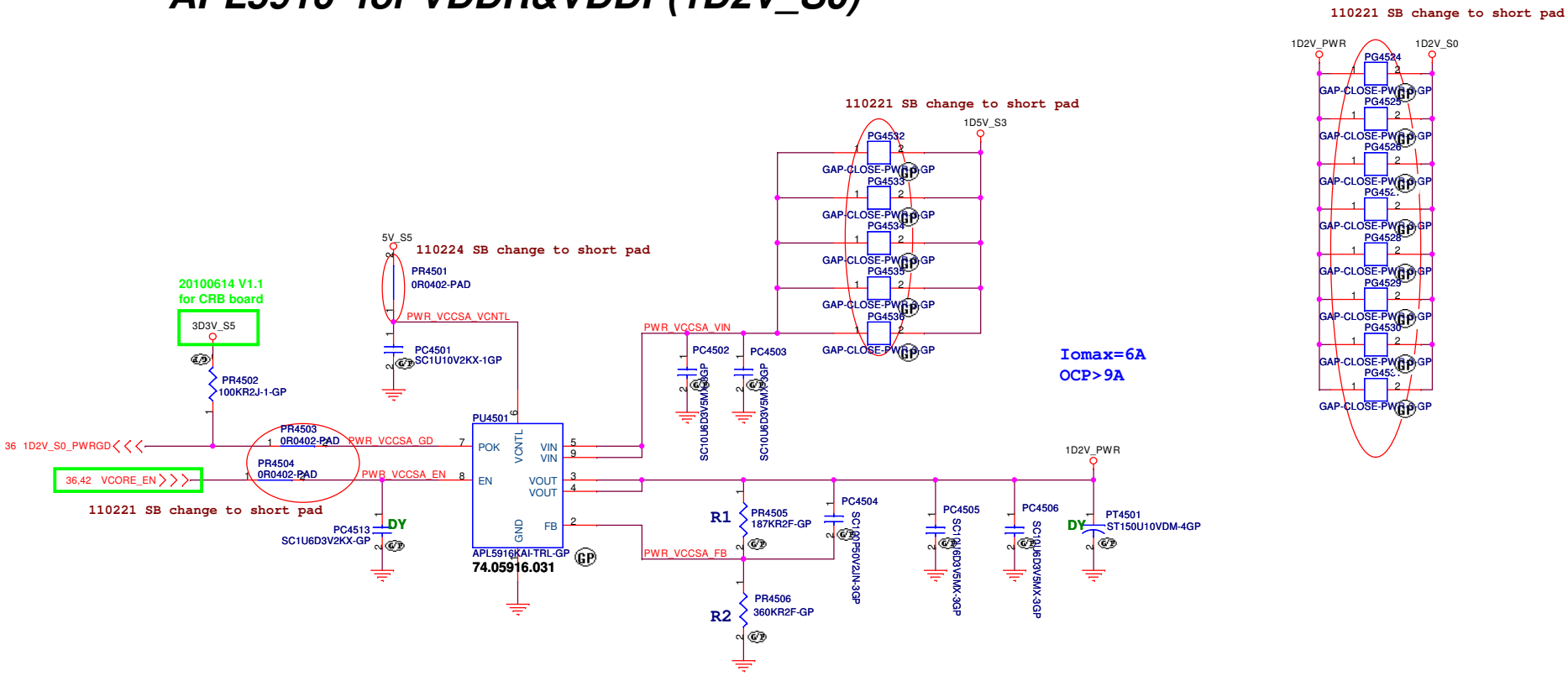
APL5916 for VDDR&VDDP(1D2V_S0)

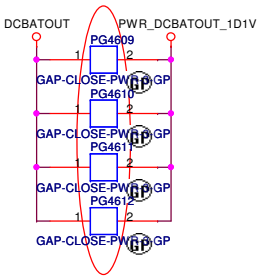


<Variant Name>

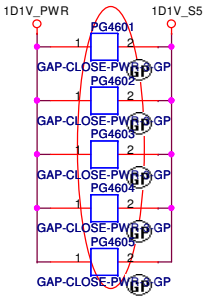
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: APL5916(1D2V_S0)		
Size: A3	Document Number: JE50 SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 45 of 102	

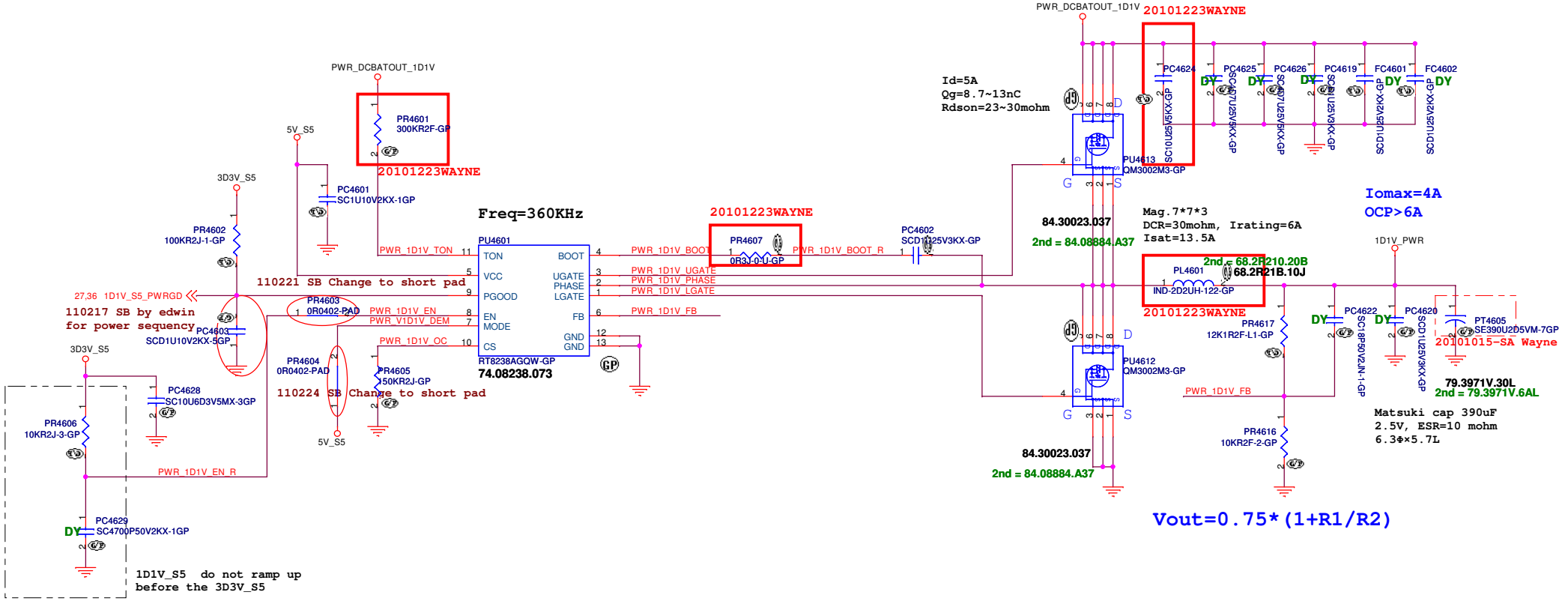
RT8238 for 1D1V_S5

110221 SB Change to short pad



110221 SB Change to short pad





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8238 (1D1V_S5)	
Size A3	Document Number JE50 SB	Rev SB
Date: Friday, April 01, 2011	Sheet 46 of 102	

(Blanking)

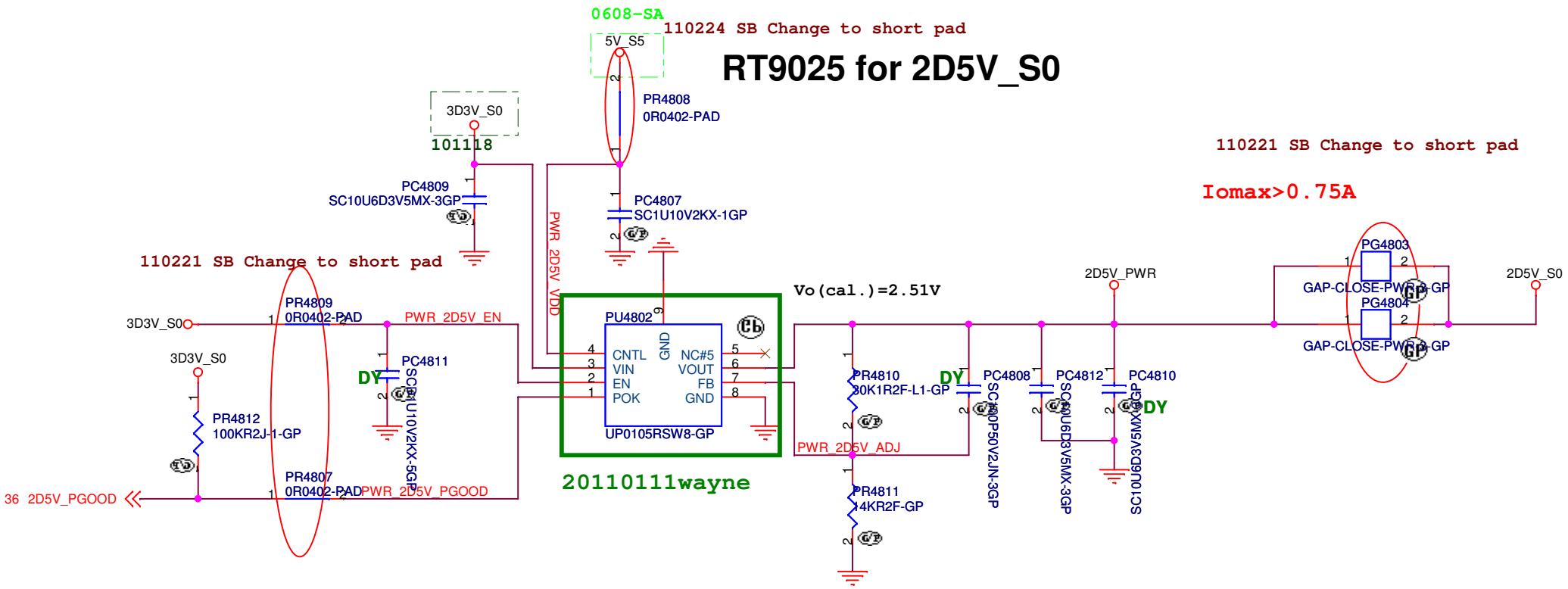
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

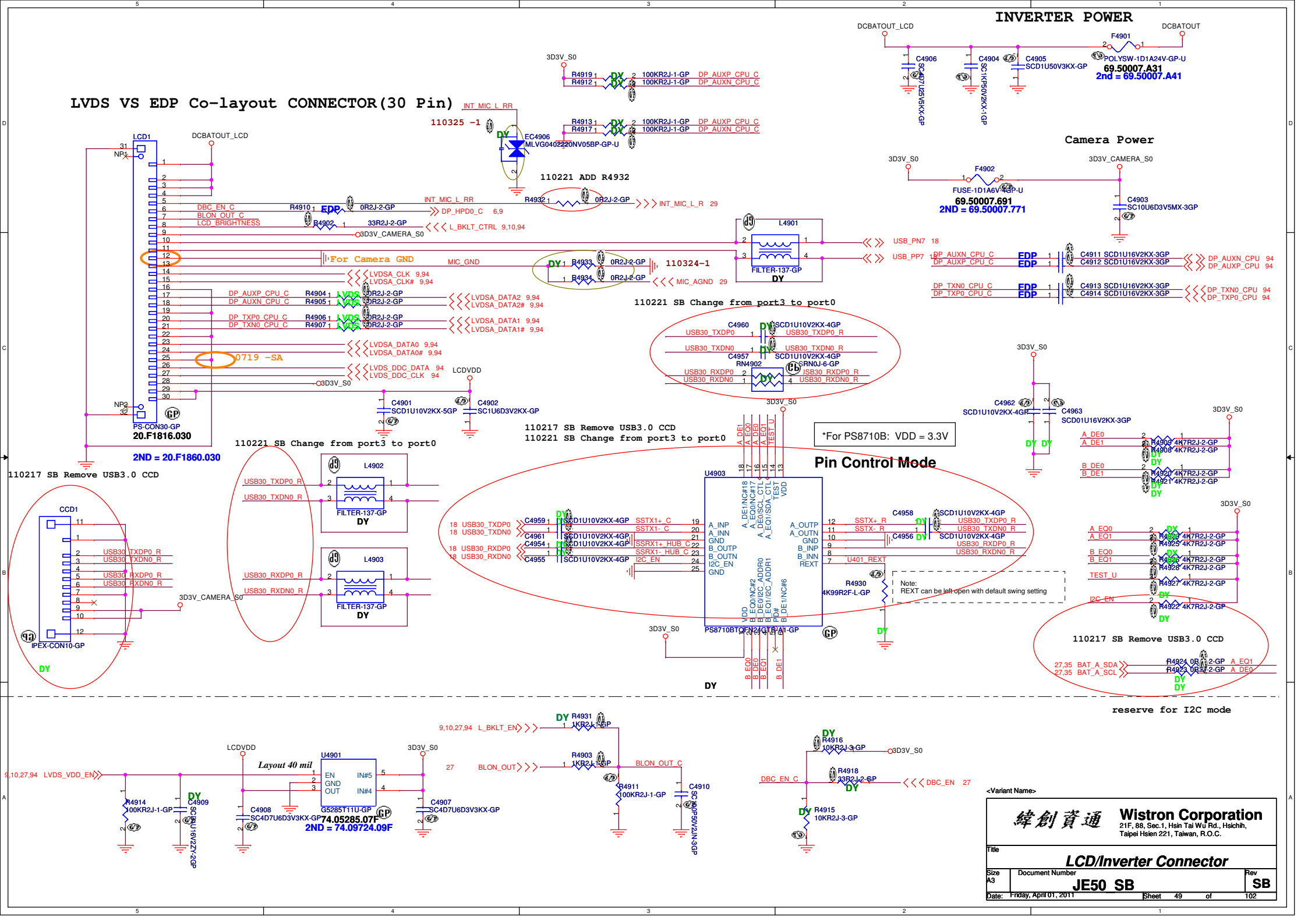
Size	Document Number	Rev
A4	JE50_SB	SB

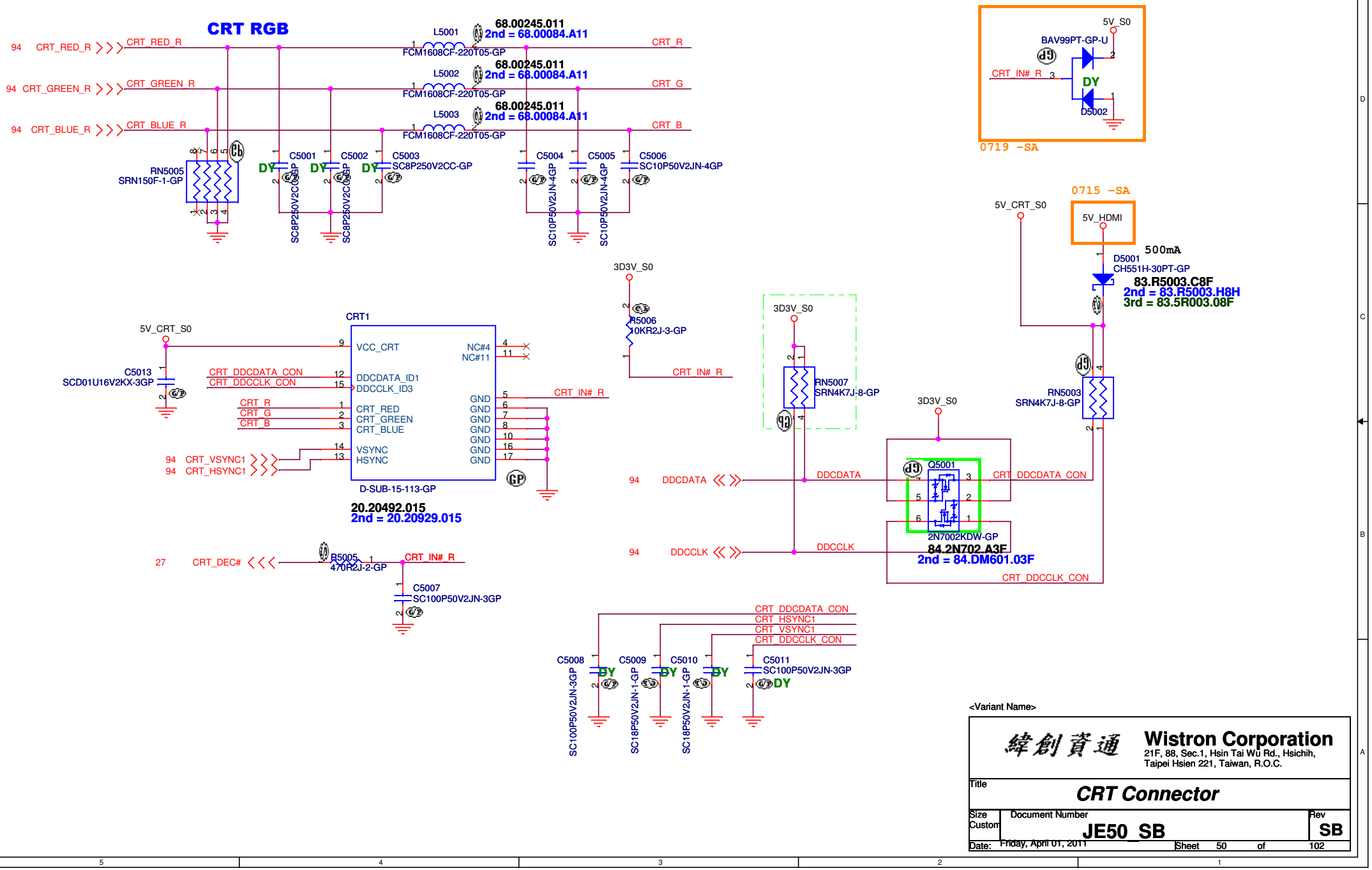
Date: Friday, April 01, 2011 Sheet 47 of 102



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RT9025(2D5V_S0)***	
Size A4	Document Number **JE50_SB**	Rev **SB**
Date: Friday, April 01, 2011	Sheet 48 of 102	


INVERTER POWER
LVDS VS EDP Co-layout CONNECTOR(30 Pin)
Camera Power
110221 ADD R4932
110324-1
110221 SB Change from port3 to port0
110217 SB Remove USB3.0 CCD
Pin Control Mode
*For PS8710B: VDD = 3.3V
reserve for I2C mode
Layout 40 mil
0719 -SA
For Camera GND
20.F1816.030
2ND = 20.F1860.030
69.50007.A31
2nd = 69.50007.A41
69.50007.691
2ND = 69.50007.771
74.05285.07F
2ND = 74.09724.09F
Note:
REXT can be left open with default swing setting
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LCD/Inverter Connector
JE50 SB
Friday, April 01, 2011



<Variant Name>

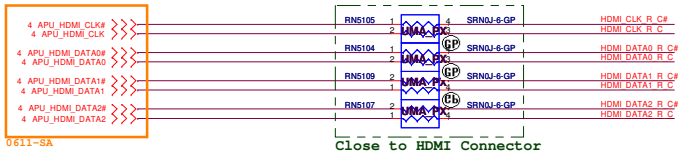
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

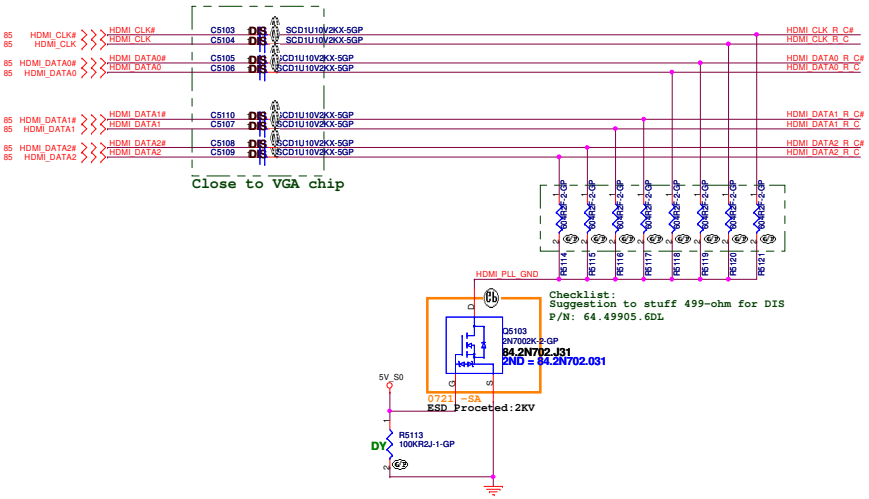
Size	Document Number	Rev
Custom	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 50 of 102

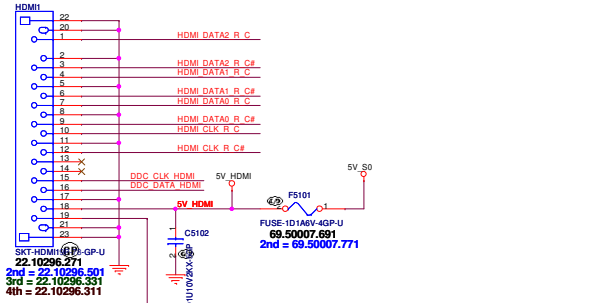
HDMI Level Shifter & CONNECTOR

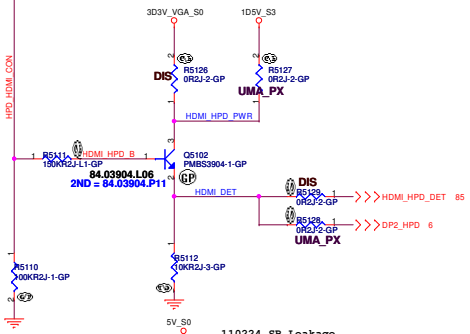


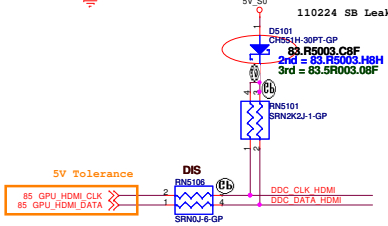
HDMI DISCRETE/ UMA Co-lay



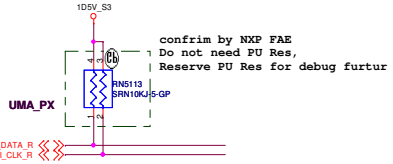
HDMI CONN

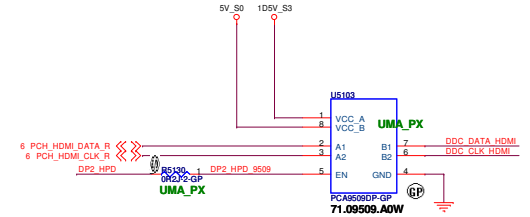


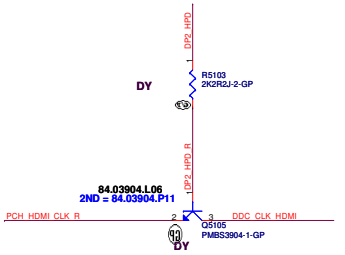


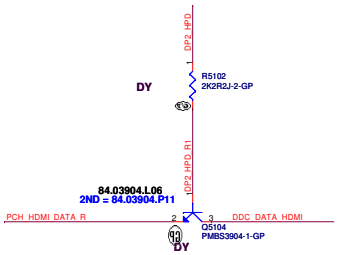


Outputs are open drain and 5-V tolerant. External pull-up resistors to
5 V are required. These signals must be pulled high (to 3.3 V or 5 V)
before VDDC is powered up.









<variant_name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI Level Shifter/Connector	
Size: A2	Document Number: JE50_SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 51 of 102	

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 52 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 53 of 102

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

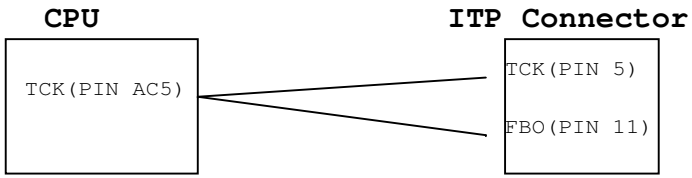
Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP

Size: A4 | Document Number: JE50_SB | Rev: SB

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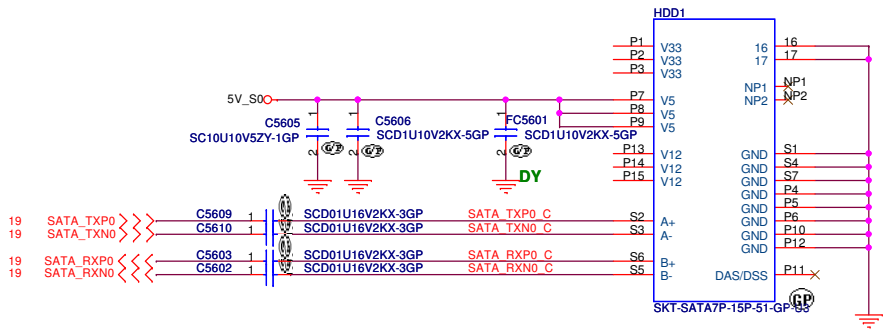
SSID = SATA

SATA HDD Connector

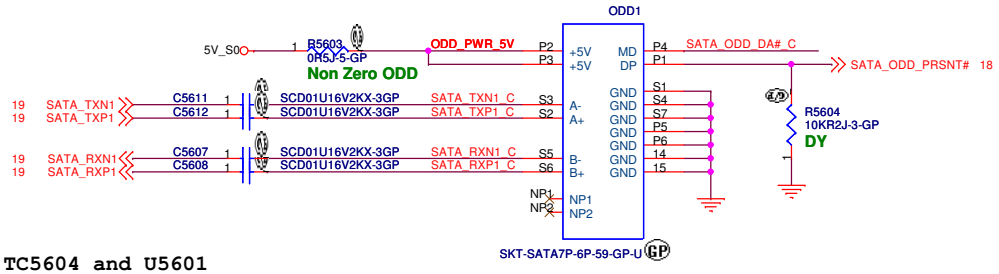


62.10065.701
2nd = 62.10065.711
3RD = 62.10065.H11

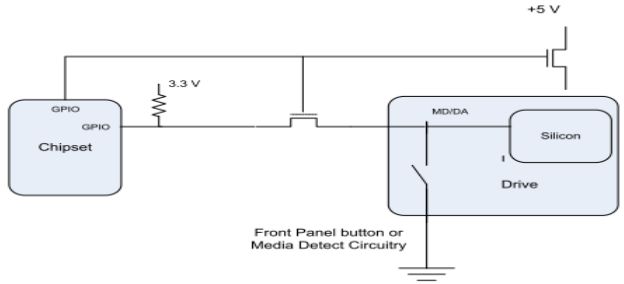
ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 10 mil

Following AMD routing table

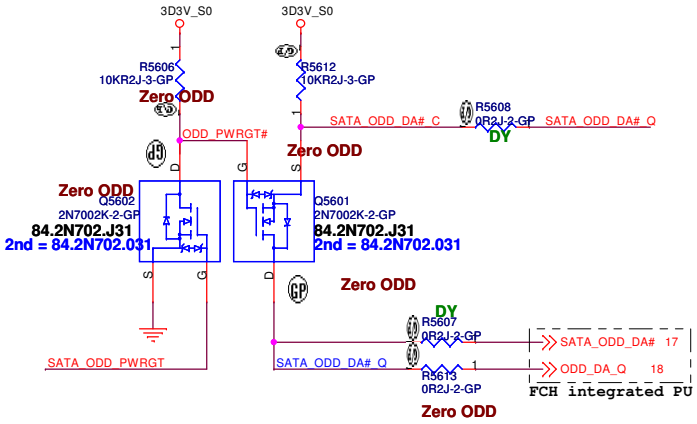


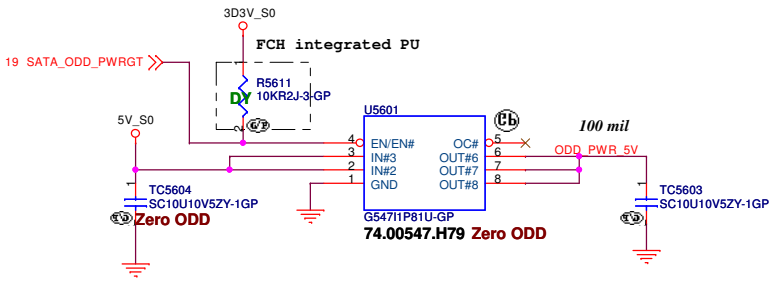
22.10300.B91
2nd = 22.10300.C21



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

If support Zero Power ODD
Stuff R5604,R5612,Q5601 and R5613 TC5604 and U5601
DY R5603





Current limit
Active High
typ =>2.5A

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 56 of 102

(Blanking)

<Variant Name>

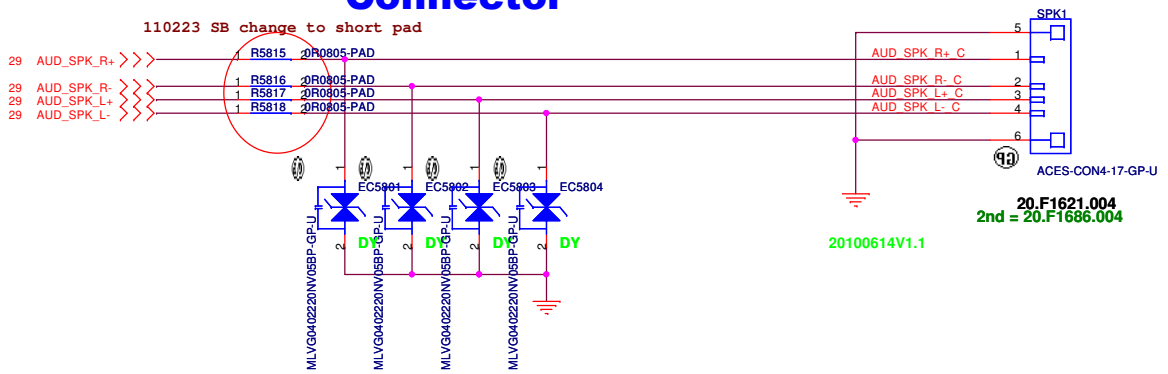
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA/USB Charger

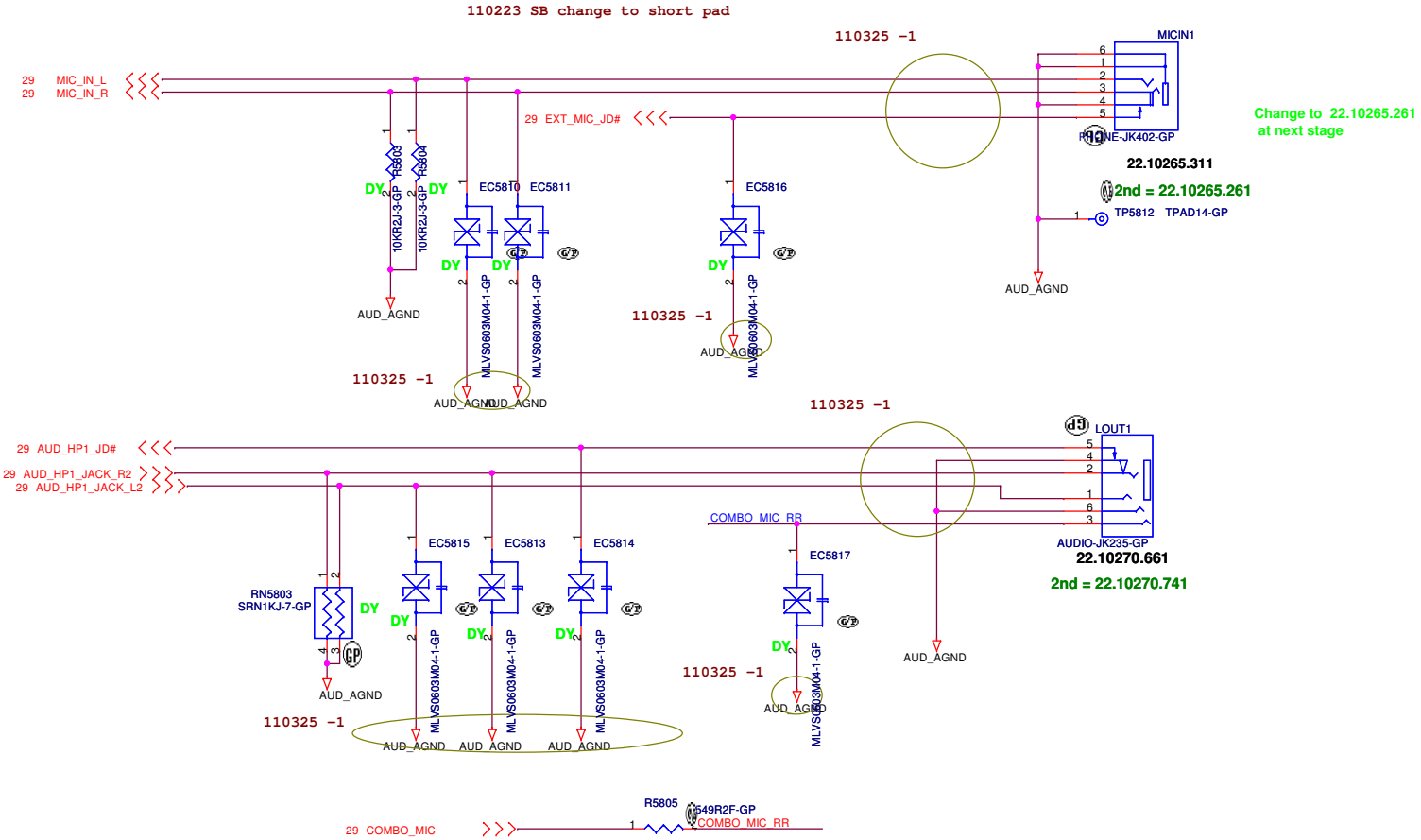
Size	Document Number	Rev
A4	JE50_SB	SB

SSID = AUDIO

Speaker Connector



MIC IN



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size	Document Number	Rev
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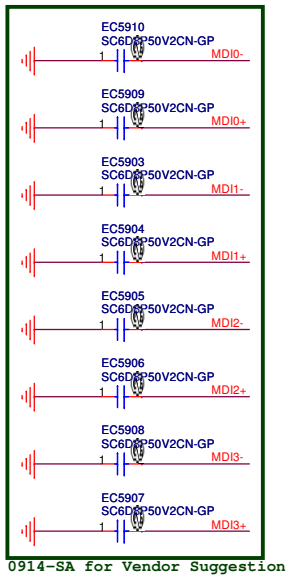
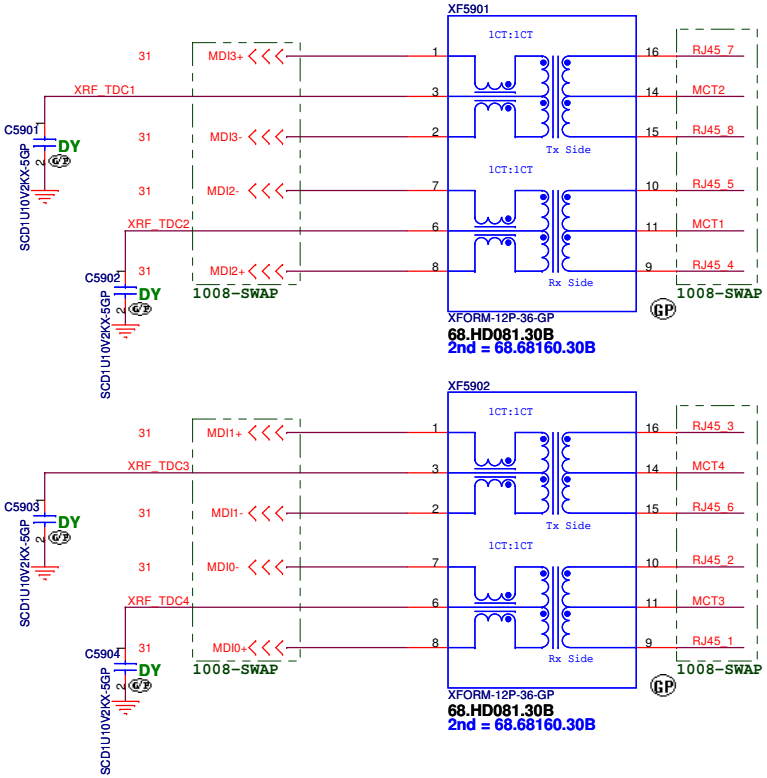
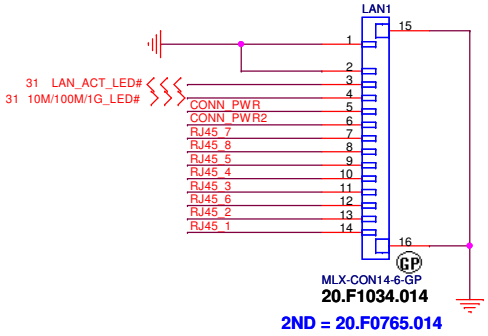
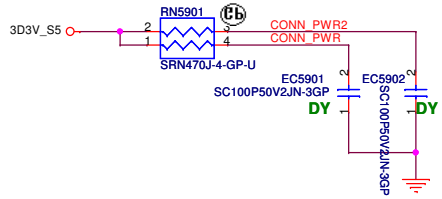


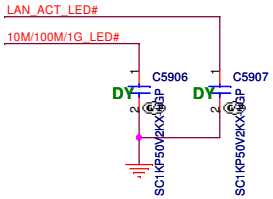
0914-SA for Vendor Suggestion

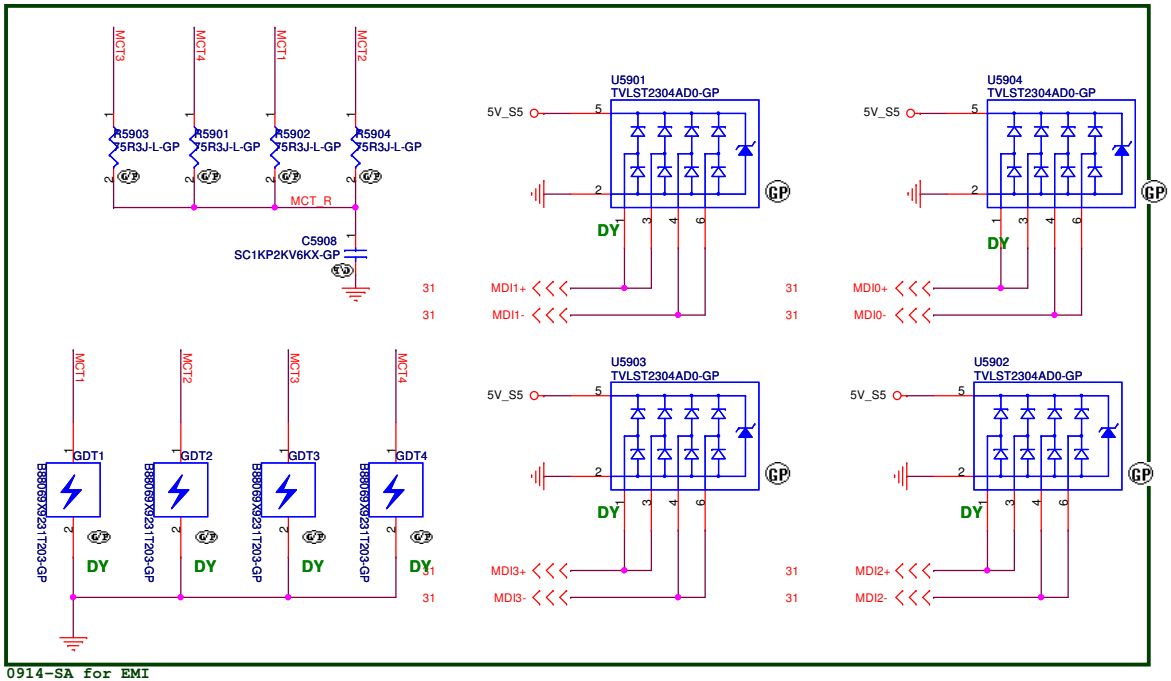
GIGA Lan Transformer











0914-SA for EMI

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN_CONN**

Size	Document Number	Rev
A3	JE50_SB	SB

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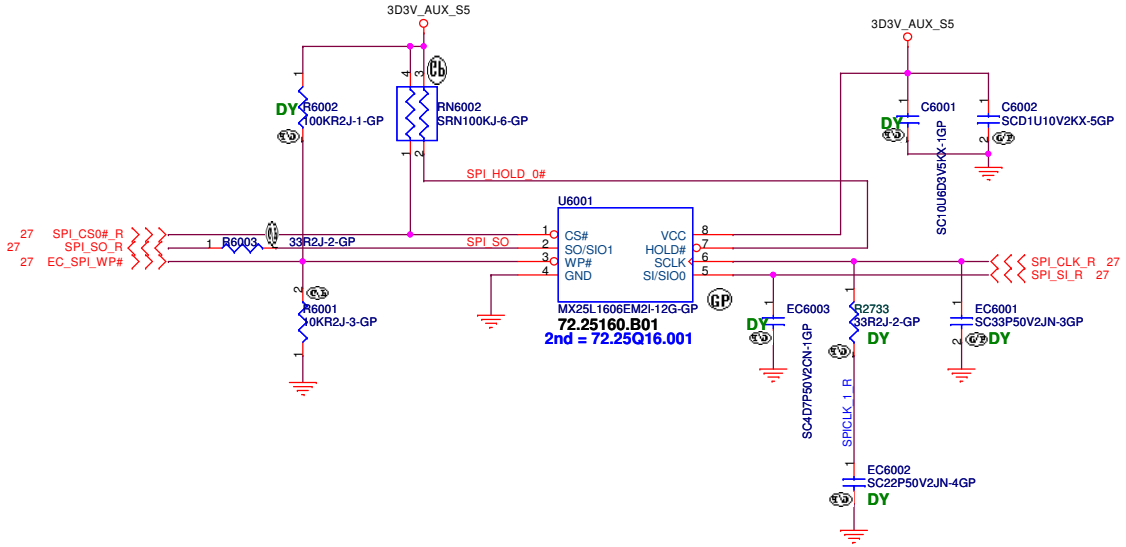
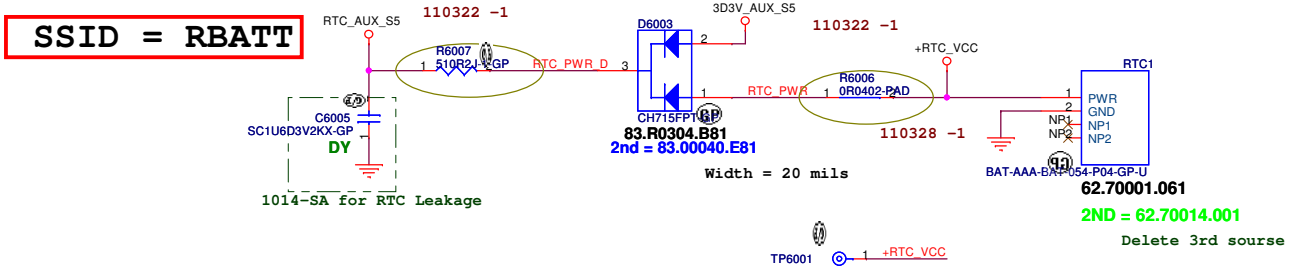
SPI FLASH ROM (2M byte) for KBC



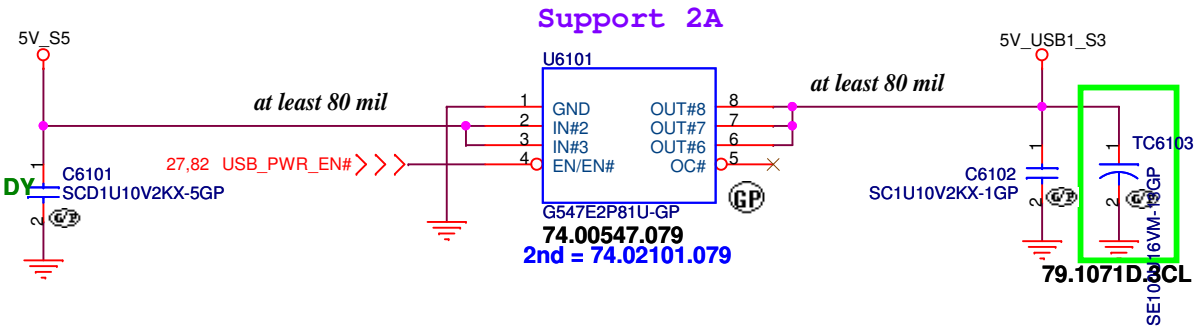
SSID = RBATT



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Flash/RTC*	
Size A3	Document Number JE50_SB	Rev SB
Date: Friday, April 01, 2011	Sheet 60 of 102	



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Power SW**

Size	Document Number	Rev
A4	JE50_SB	SB

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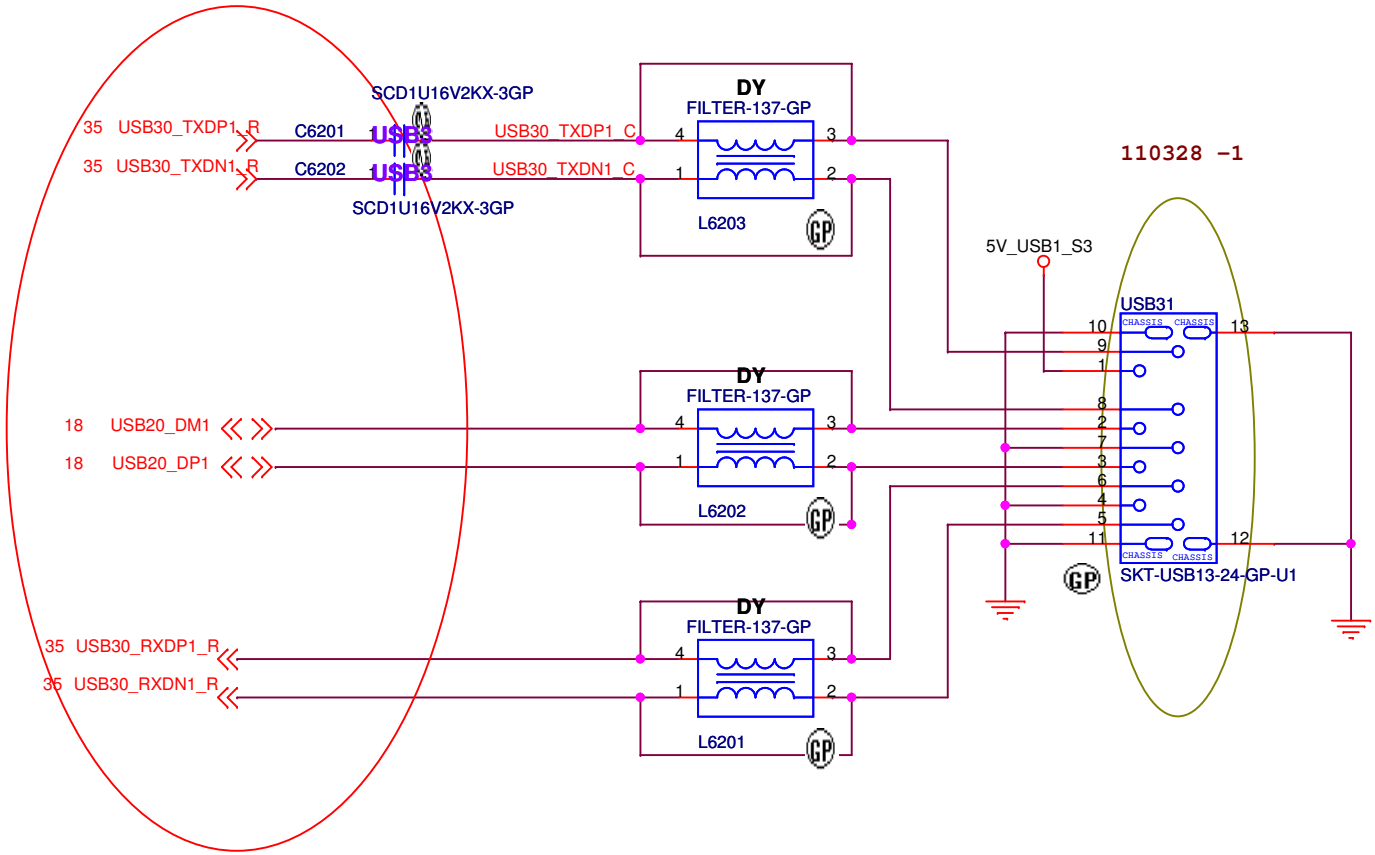
110221 SB Change from port2 to port1



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0

Size	Document Number	Rev
A4	JE50_SB	SB

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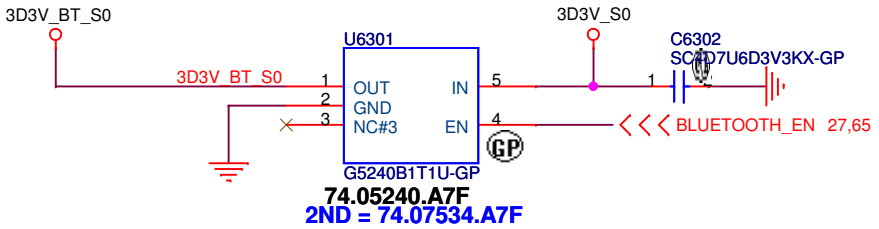
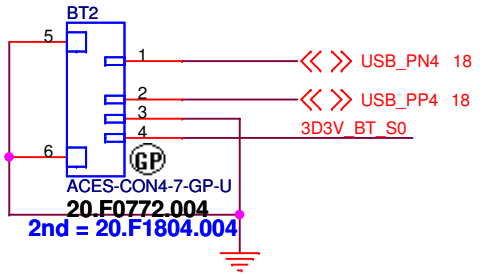
ANNIE Bluetooth Module

1.5A / High Active Voltage 2V





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLUE TOOTH**		
Size: A4	Document Number: **JE50_SB**	Rev: **SB**
Date: Friday, April 01, 2011	Sheet 63 of 102	

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

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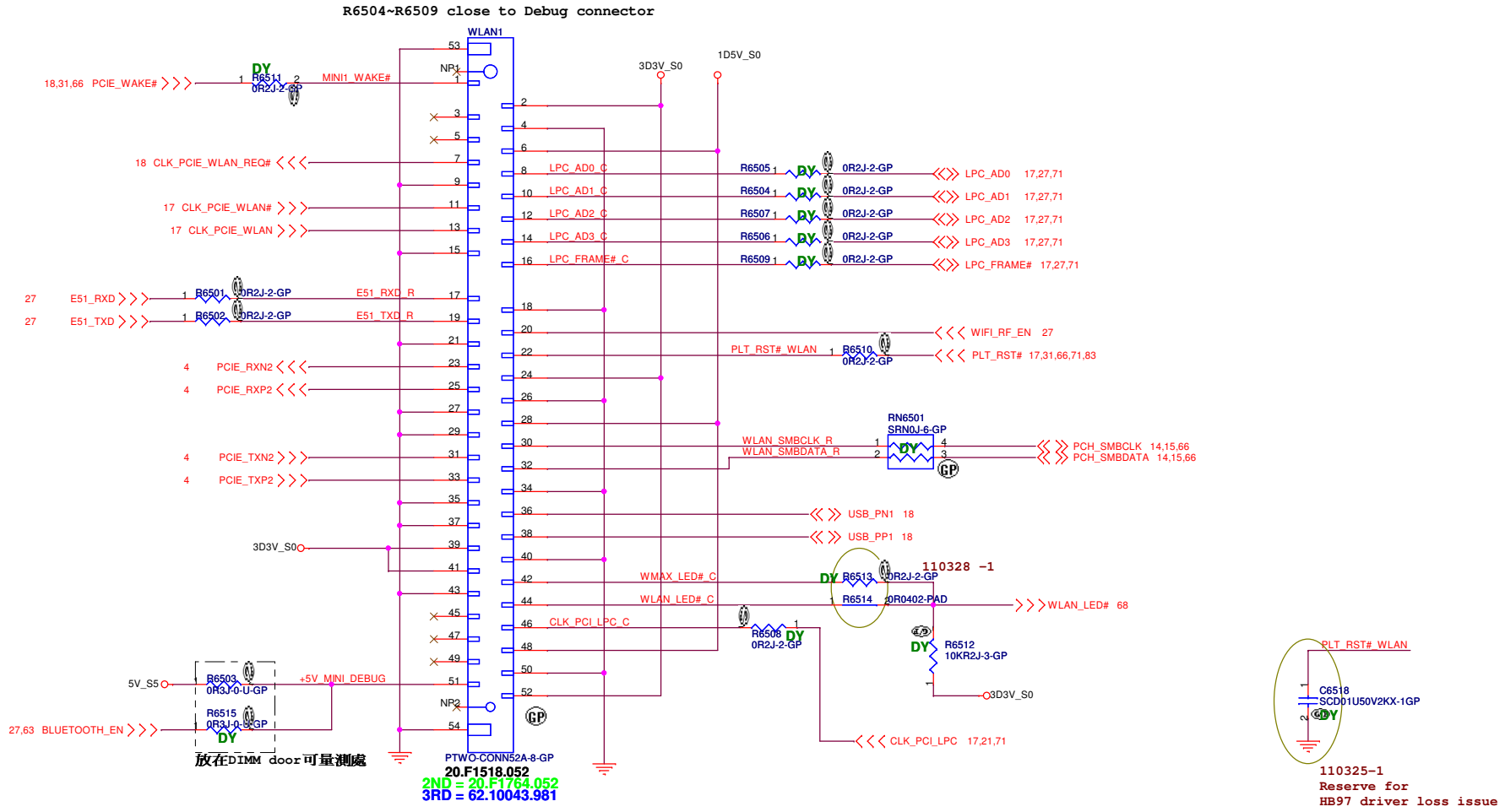
Mini Card Connector(802.11a/b/g/n)



<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: WLAN		
Size: A3	Document Number: JE50_SB	Rev: SB
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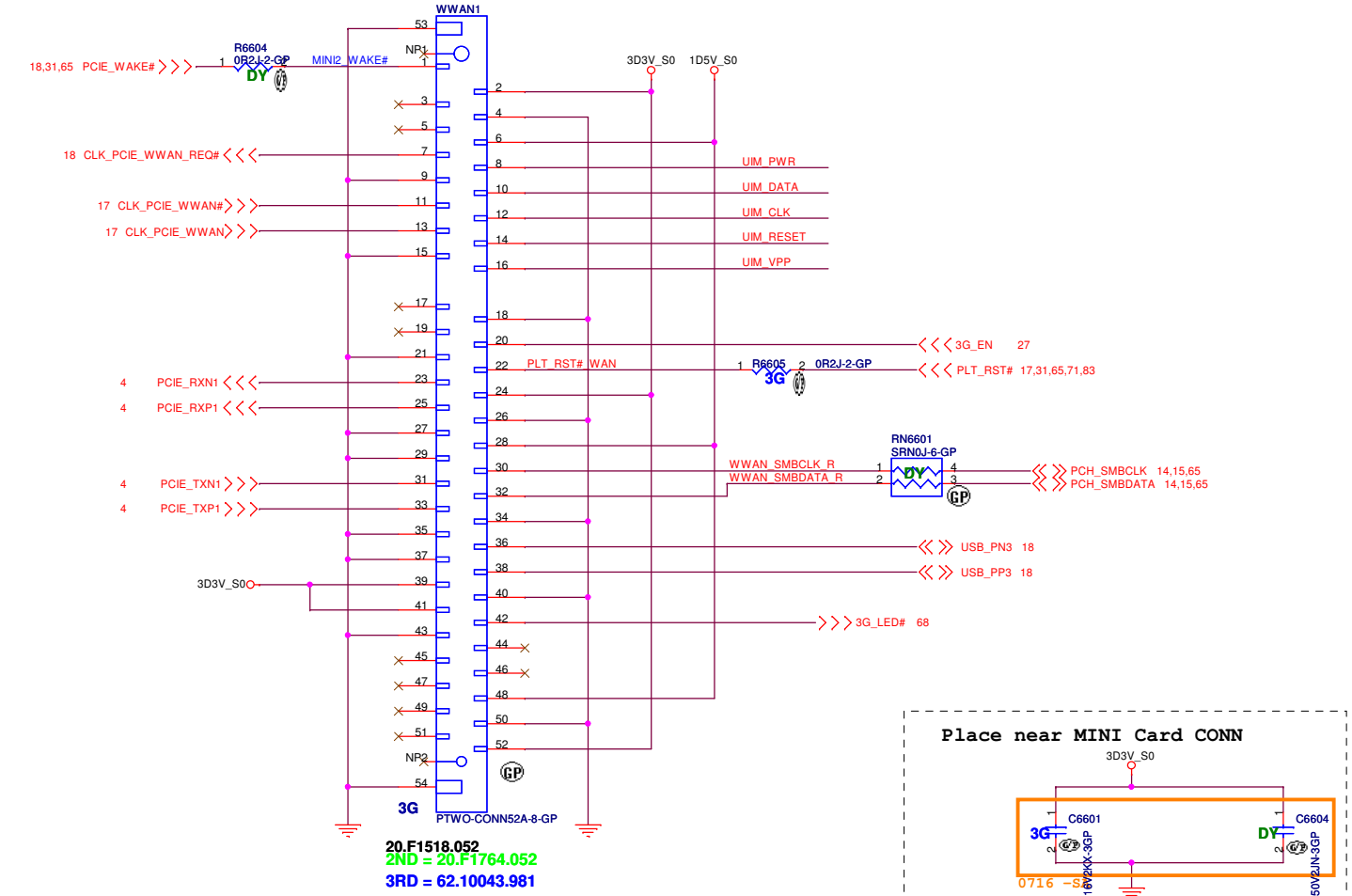
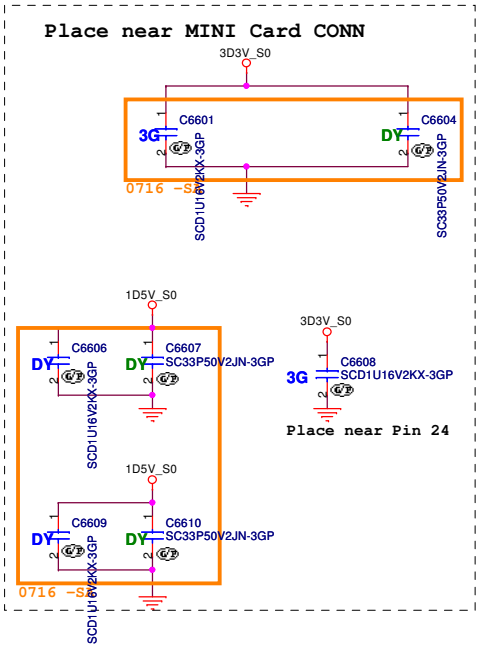
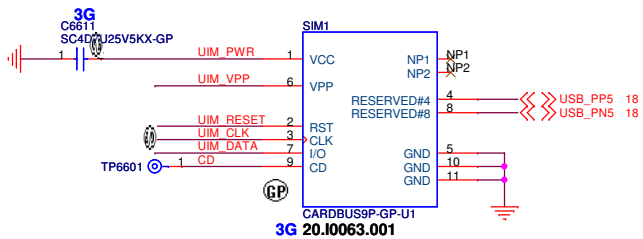
Mini Card Connector(WWAN)







<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN

Size	Document Number	Rev
A3	JE50 SB	SB

Date: Friday, April 01, 2011 Sheet 66 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

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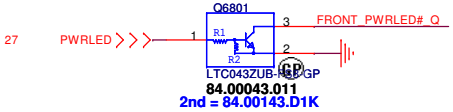
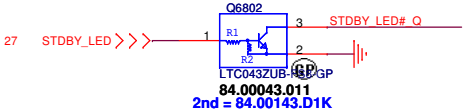
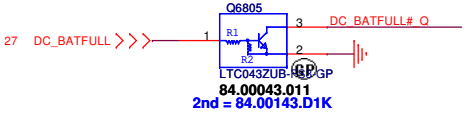
Power button LED



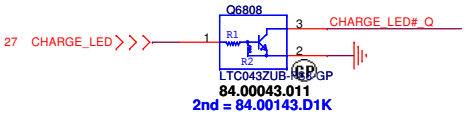
Power STDBY_LED

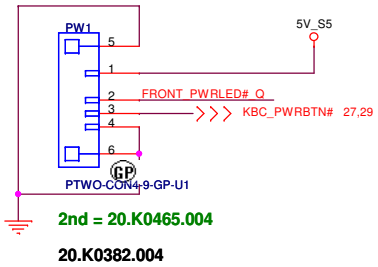


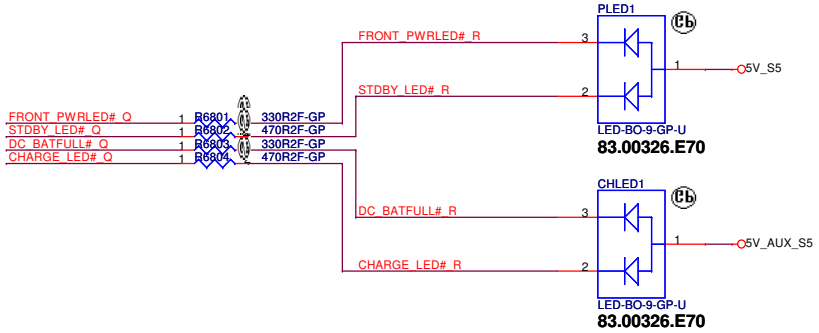
Battery LED2 (DC_BATFULL)

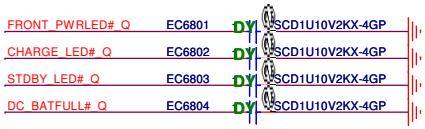


Battery LED1 (CHARGE)

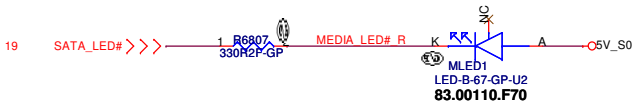


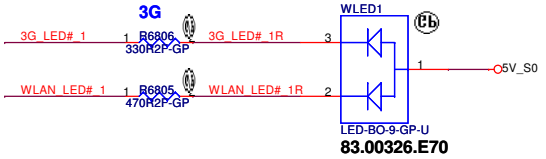




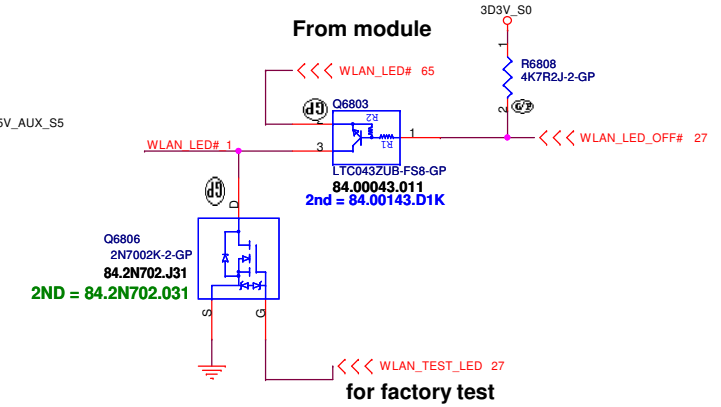


SATA HDD LED

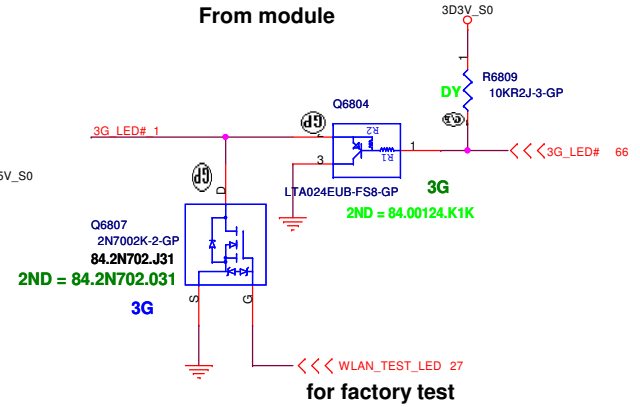




WLAN_LED



3G LED



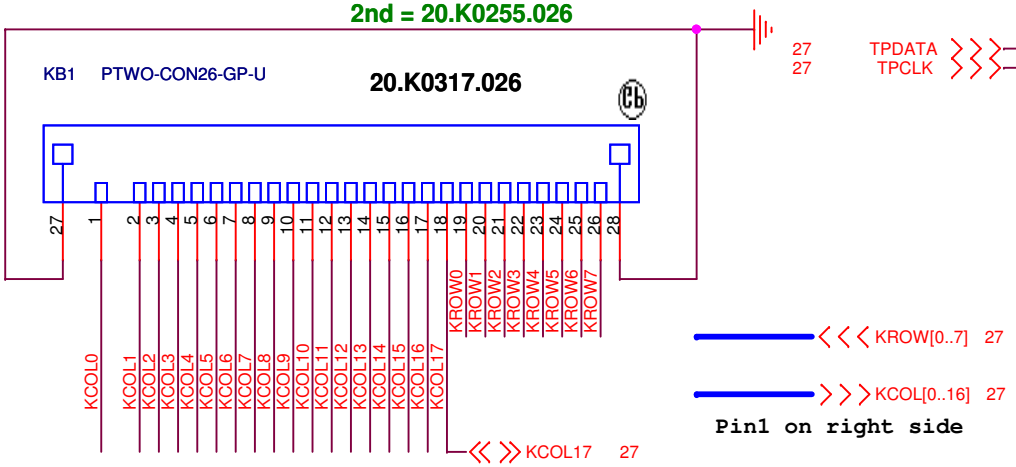
<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LED Bard/Power Button		
Size: A3	Document Number: JE50 SB	Rev: SB
Date: Friday, April 01, 2011	Sheet 68 of 102	

Internal KeyBoard Connector

2nd = 20.K0255.026

KB1 PTWO-CON26-GP-U 20.K0317.026



27
27
TPDATA
TPCLK

KROW[0..7] 27

KCOL[0..16] 27

KCOL17 27

Pin1 on right side

MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

1 K/B 26

TOUCH PAD

5V_S0

RN6901
SRN4K7J-8-GP

EC6901
SCD1U10V2KX-4GP
DY

EC6902
SCD1U10V2KX-4GP

20.K0315.012
2nd = 20.K0370.012

TPAD1
ACES-CON12-9-GP-U

SRN33J-5-GP-U
RN6902

TPDATA
TPCLK
TP_DATA
TP_CLK

TP_DATA
TP_CLK
TP_LEFT
TP_RIGHT

EC6903 SC100P50V2JN-3GP
EC6904 SC100P50V2JN-3GP
EC6905 SC100P50V2JN-3GP
EC6906 SC100P50V2JN-3GP

1 T/P 12

SW_R1
SW-TACT-5P-9-GP
62.40089.221

SW_L1
SW-TACT-5P-9-GP
62.40089.221

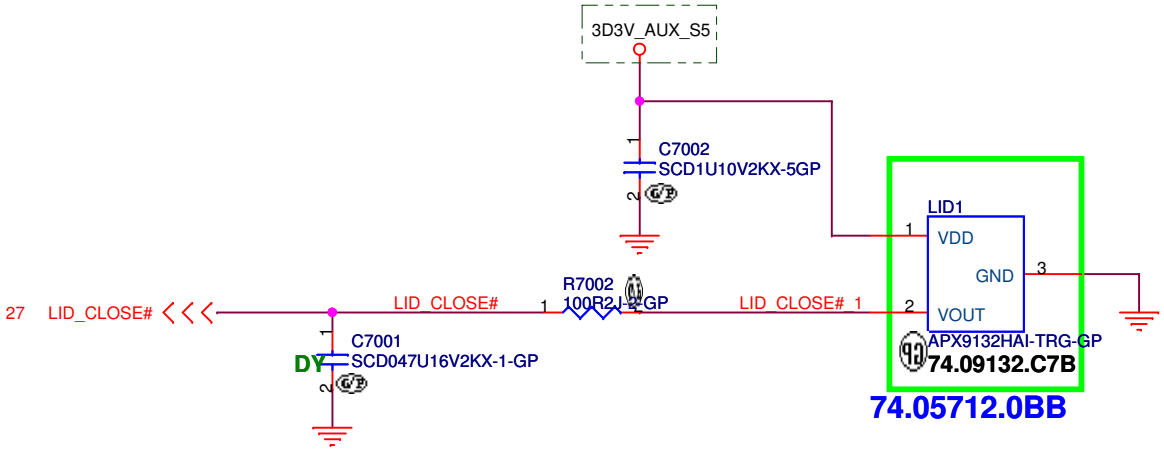
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 69 of 102



<Variant Name>

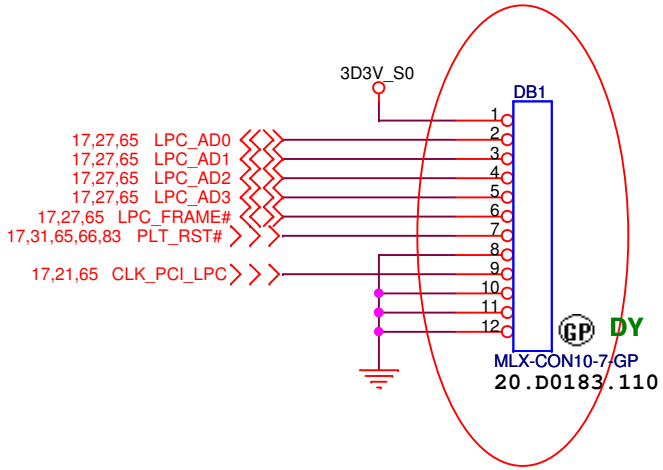
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

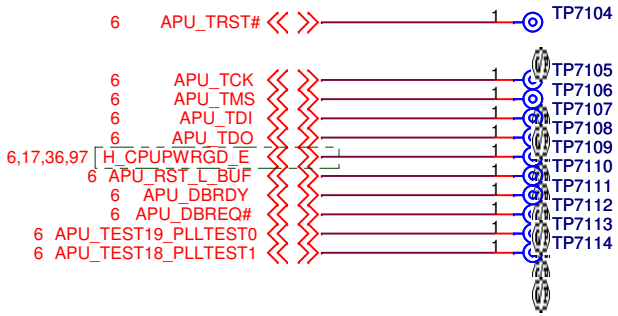
Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 70 of 102

110218 SB BOM Change



HDT+ Connectors



CRB:placed 0-ohm
Checklist: If both SCAN and HDT+ header are implement
placed 15-ohm

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 71 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 72 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

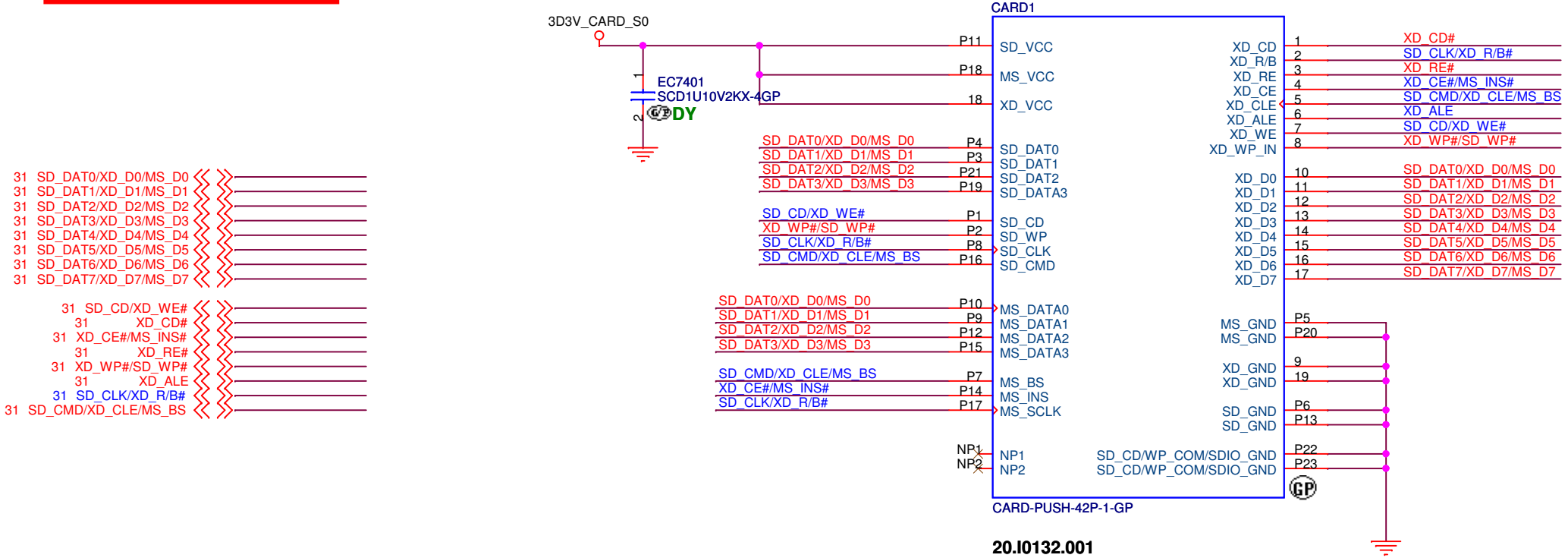
Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 73 of 102

SD/XD/MS Card Reader

SSID = SDIO



Pin No.	SD/MMC	MS/MS PRO	xD
P1	xD-R/B		2P
P2	xD-RE		3P
P3	xD-CE		4P
P4	xD-CLE		5P
P5	xD-ALE		6P
P6	xD-WE		7P
P7	xD-WP		8P
P8	xD-D0		10P
P9	xD-D1		11P
P10	SD-DAT2	9P	
P11	SD-DAT3	1P	
P12	SD-CMD	2P	
P13	4in1-GND	3P/6P	1P/10P 1P/9P
P14	MS-VCC		9P
P15	MS-SCLK		8P
P16	MS-DATA3		7P
P17	MS-INS		6P
P18	MS-DATA2		5P
P19	MS-DATA0		4P

Pin No.	SD/MMC	MS/MS PRO	xD
P20	MS-DATA1	3P	
P21	MS-BS	2P	
P22	4in1-GND	3P/6P	1P/10P 1P/9P
P23	SD-VCC	4P	
P24	SD-CLK	5P	
P25	SD-DAT0	7P	
P26	xD-D2		12P
P27	xD-D3		13P
P28	xD-D4		14P
P29	SD-DAT1	8P	
P30	xD-D5		15P
P31	xD-D6		16P
P32	xD-D7		17P
P33	xD-VCC		18P
P34	XD-CD-SW		19P
P35	SD-WP-SW	SD-WP-SW	
P36	SD-CD-SW	SD-CD-SW	
P37 P38	4 IN 1-GND	SD-WP/CD-SW-GND	

<Variant Name>

Card-reader Off-Page

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 74 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 75 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 76 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 77 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 78 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 79 of 102

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 80 of 102

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<Variant Name>

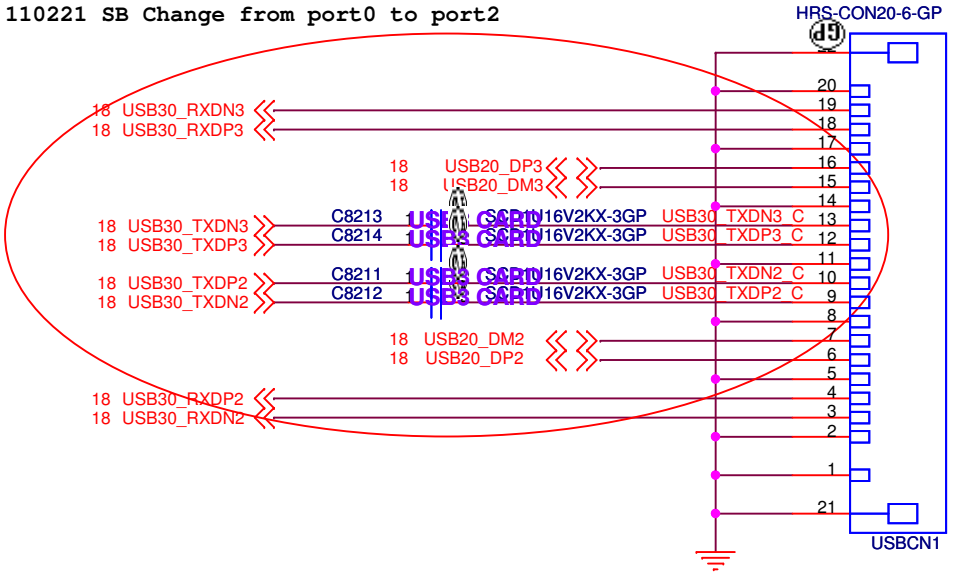
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE50_SB	SB

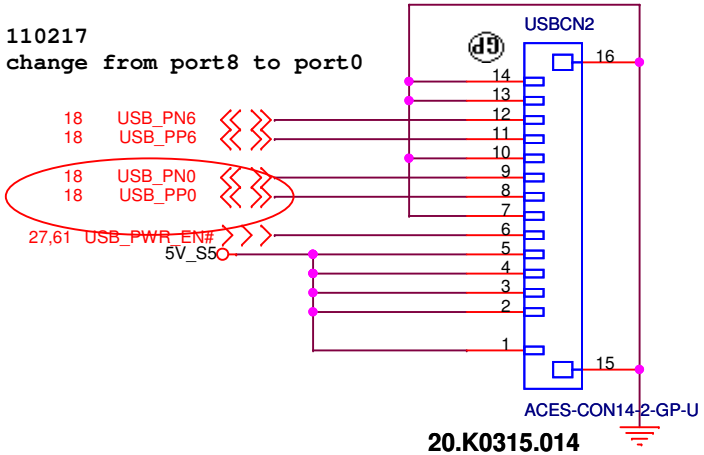
Date: Friday, April 01, 2011 Sheet 81 of 102

110221 SB Change from port1 to port3
110221 SB Change from port0 to port2



USB3 CARD

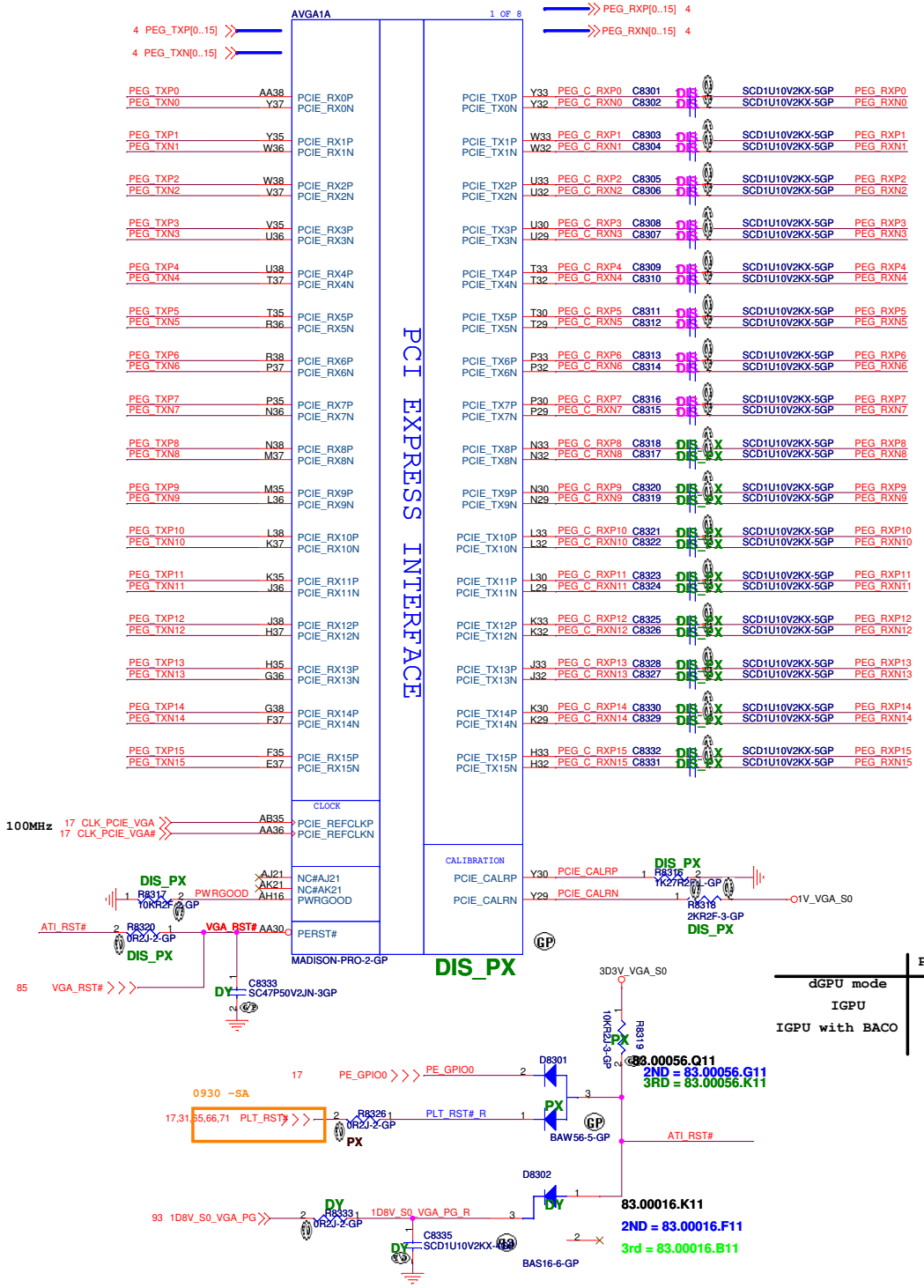
110217
change from port8 to port0



20.K0315.014
2nd = 20.K0370.014

<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	IO Board Connector	
Size A4	Document Number JE50_SB	Rev SB
Date: Friday, April 01, 2011	Sheet 82 of 102	



CONFIGURATION STRAPS

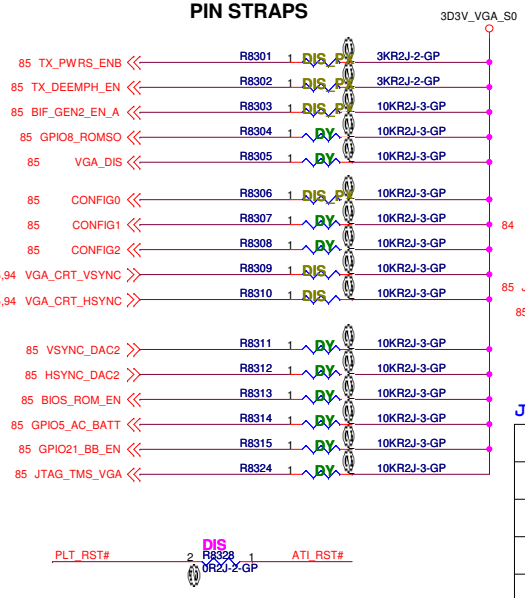
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

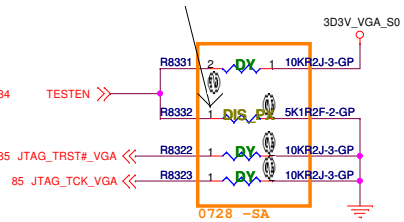
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACO	H

PIN STRAPS



R8332 stuff 1K for Mannhatton VGA
stuff 5.1K for Vancouver VGA



JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

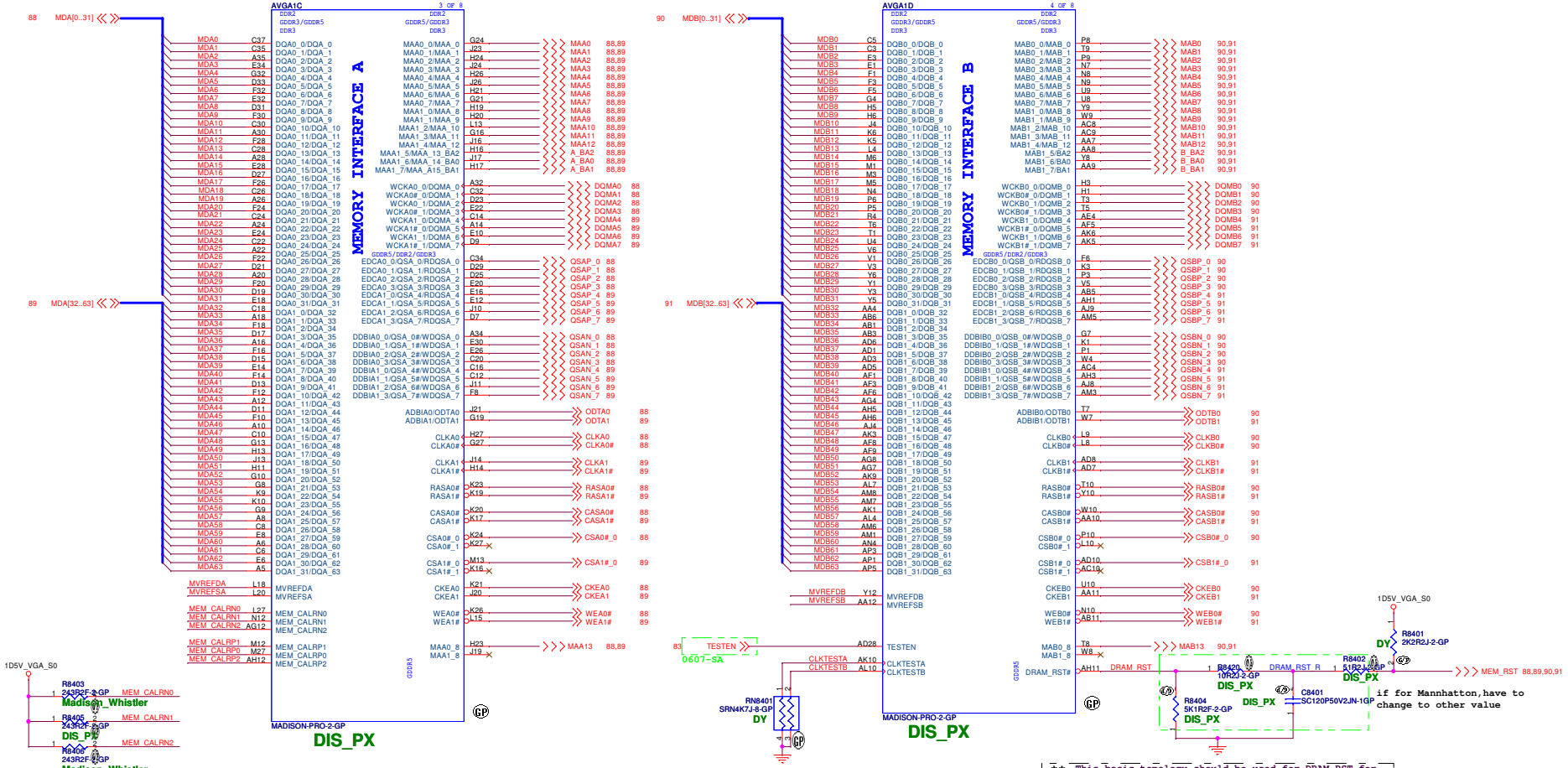
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size: Custom | Document Number: JE50_SB | Rev: SB

Date: Friday, April 01, 2011 | Sheet 83 of 102



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

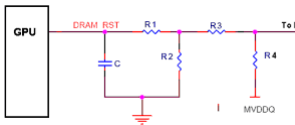
Vancouver

C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Mannhatton



C	R1	R2	R3	R4
68 pF	51 Ω	10 kΩ	0 Ω	DNI

<variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_Memory(2/5)

Size: Custom | Document Number: JE50_SB | Rev: SB

Date: Friday, April 01, 2011 | Sheet 84 of 102

DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request

Address	DVPDATA[3:0]	Vender	PN	Speed	
0	0 0 0 0	Hynix	H5TQ1G63DFR-11C 1Gb(64Mx16)	900Mhz	Rev D Die NEW ! !
1	0 0 0 1	Hynix	H5TQ2G63BFR-11C 2Gb(128Mx16)	900Mhz	Rev B Die
2	0 0 1 0	Reserve			
3	0 0 1 1	Hynix	H5TQ1G63DFR-12C 1Gb(64Mx16)	800Mhz	Rev D Die NEW ! !
4	0 1 0 0	Hynix	H5TQ1G63BFR-12C 1Gb(64Mx16)	800Mhz	Rev B Die
5	0 1 0 1	Reserve			
6	0 1 1 0	Reserve			
7	0 1 1 1	Hynix	H5TQ2G63BFR-11C 2Gb(128Mx16)	800Mhz	Rev B Die
8	1 0 0 0	Samsung	K4W1G1646E-HC12 1Gb(64Mx16)	800Mhz	Rev E Die
9	1 0 0 1	Samsung	K4W2G1646C-HC11 2Gb(128Mx16)	900Mhz	Rev C Die NEW ! !
10	1 0 1 0	Reserve			
11	1 0 1 1	Samsung	K4W2G1646B-HC12 2Gb(128Mx16)	800Mhz	Rev B Die
12	1 1 0 0	Samsung	K4W1G1646G-BC11 1Gb(64Mx16)	900Mhz	Rev G Die NEW ! !
13	1 1 0 1	Reserve			
14	1 1 1 0	ATI	23EY4187MA11 2GB(128M*16)	900Mhz	NEW ! !
15	1 1 1 1	Samsung	K4W1G1646G-BC12 1Gb(64Mx16)	800Mhz	Rev G Die NEW ! !

Apollo use Hynix D die 1GB 900MHz

LVDS Interface

I2C Bus for LVDS

Straps

For new version no 27M

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

DDC1/DDC2/DDC6 have 5V-tolerant

DDC1 channel for CRT

DDC2 channel for HDMI

AUXP PD 100K
AUXN PU 100K
Draw on EDP circuit page

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

0719 -SA

1022-SA
Use same parts for VGA DPPower

1022-SA Delete

1022-SA
TM Derek Hsieh suggestion

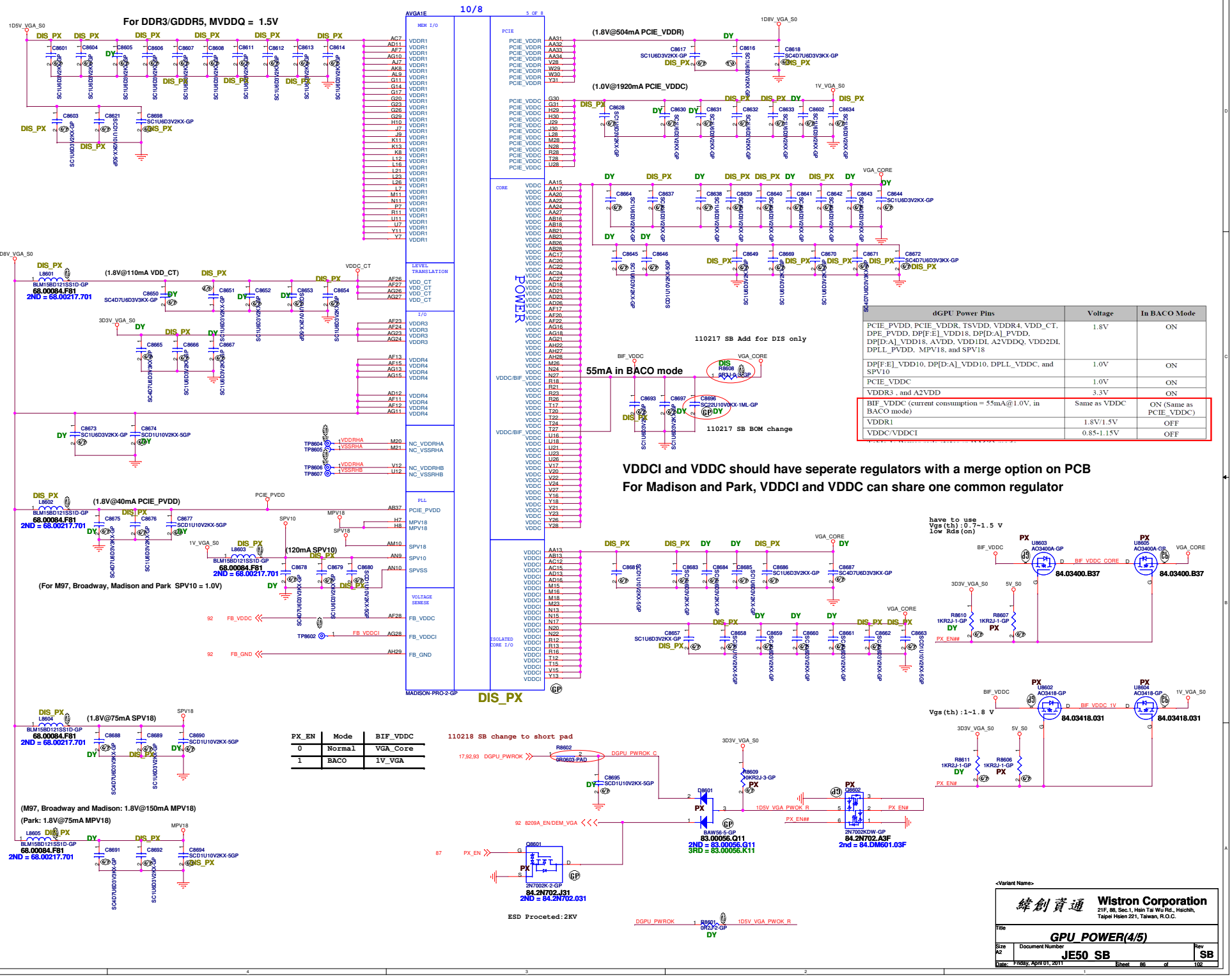
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size	Document Number	Rev
A2	JE50_SB	SB

Date: Friday, April 01, 2011 Sheet 85 of 102



dGPU Power Pins	Voltage	In BACO Mode
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	ON
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	ON
PCIE_VDDC	1.0V	ON
VDDR3 , and A2VDD	3.3V	ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	ON (Same as PCIE_VDDC)
VDDR1	1.8V/1.5V	OFF
VDDC/VDDCI	0.85~1.15V	OFF

PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

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Title: GPU_POWER(4/5)

Size: A2 | Document Number: JE50_SB | Rev: SB

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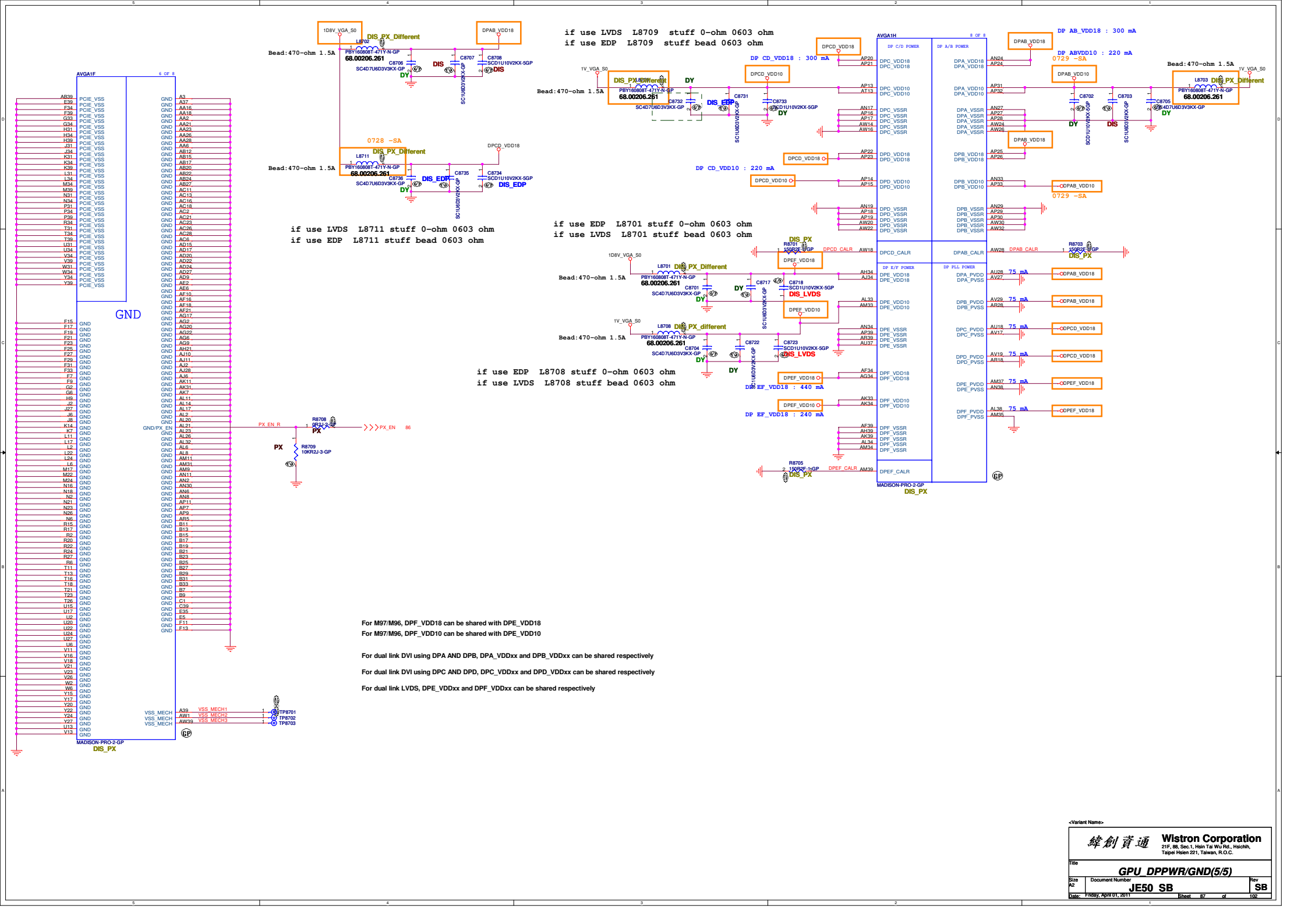

For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
For M97/M96, DPF_VDD10 can be shared with DPE_VDD10

For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively

For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively

For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively

<Variant Name>

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Title: ***GPU_DPPWR/GND(5/5)***

Size	Document Number	Rev
A2	JE50 SB	SB

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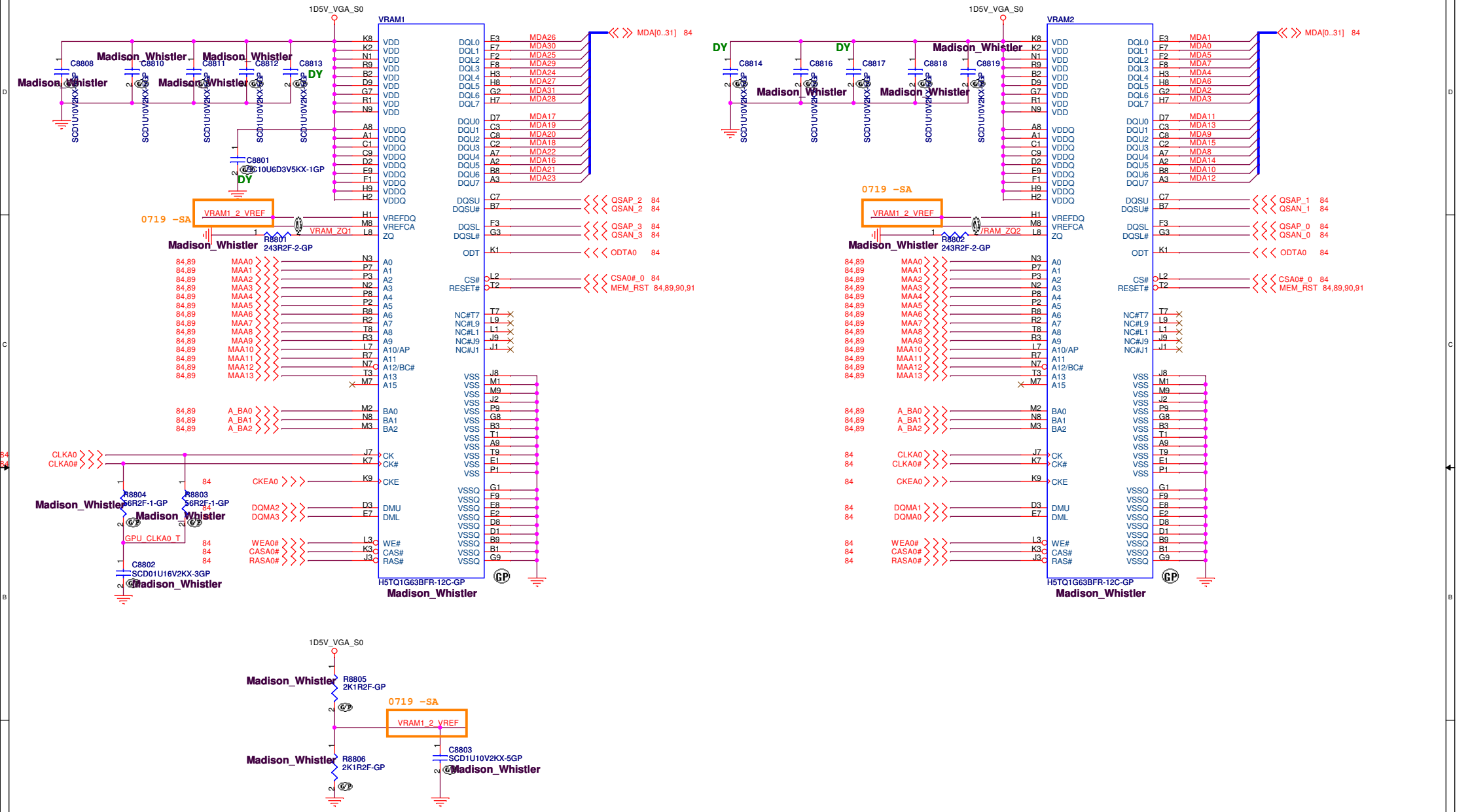
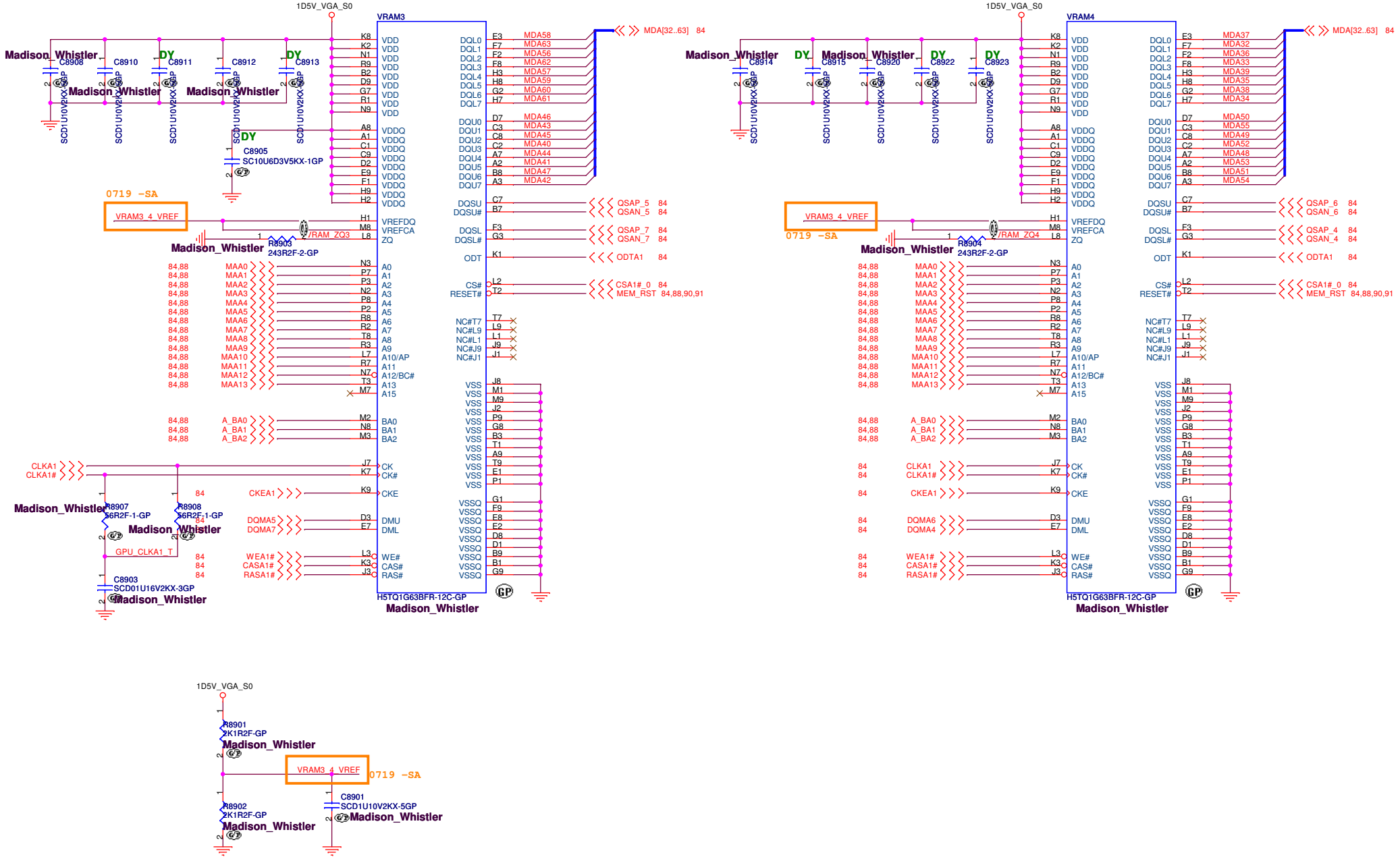


<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU-VRAM1,2 (1/4)***
Size A3	Document Number **JE50 SB** Rev **SB**
Date: Friday, April 01, 2011	Sheet 88 of 102



<Variant Name>

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Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
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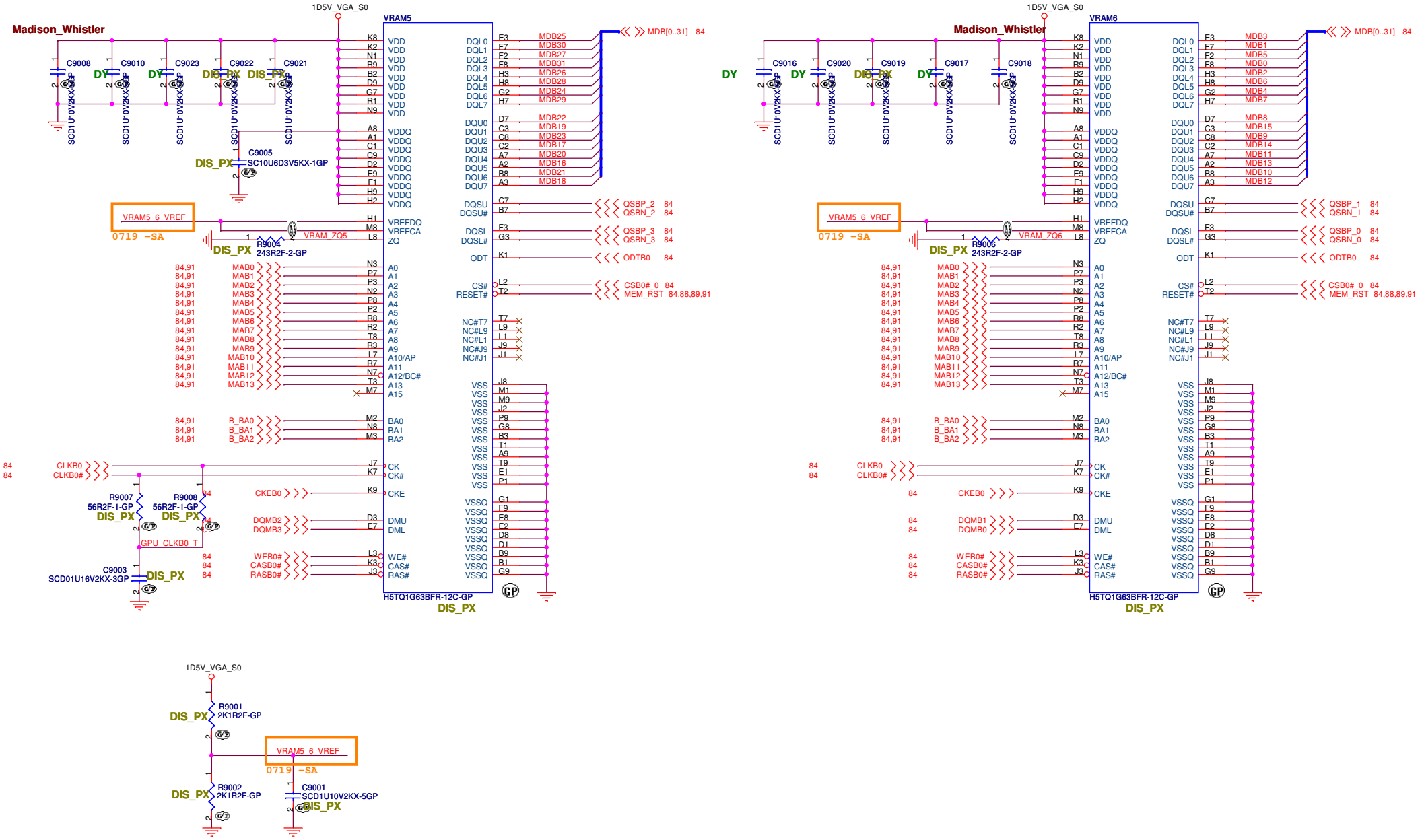

<Variant Name>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU-VRAM5,6 (3/4)
Size A3 / Document Number	JE50_SB
Rev	SB
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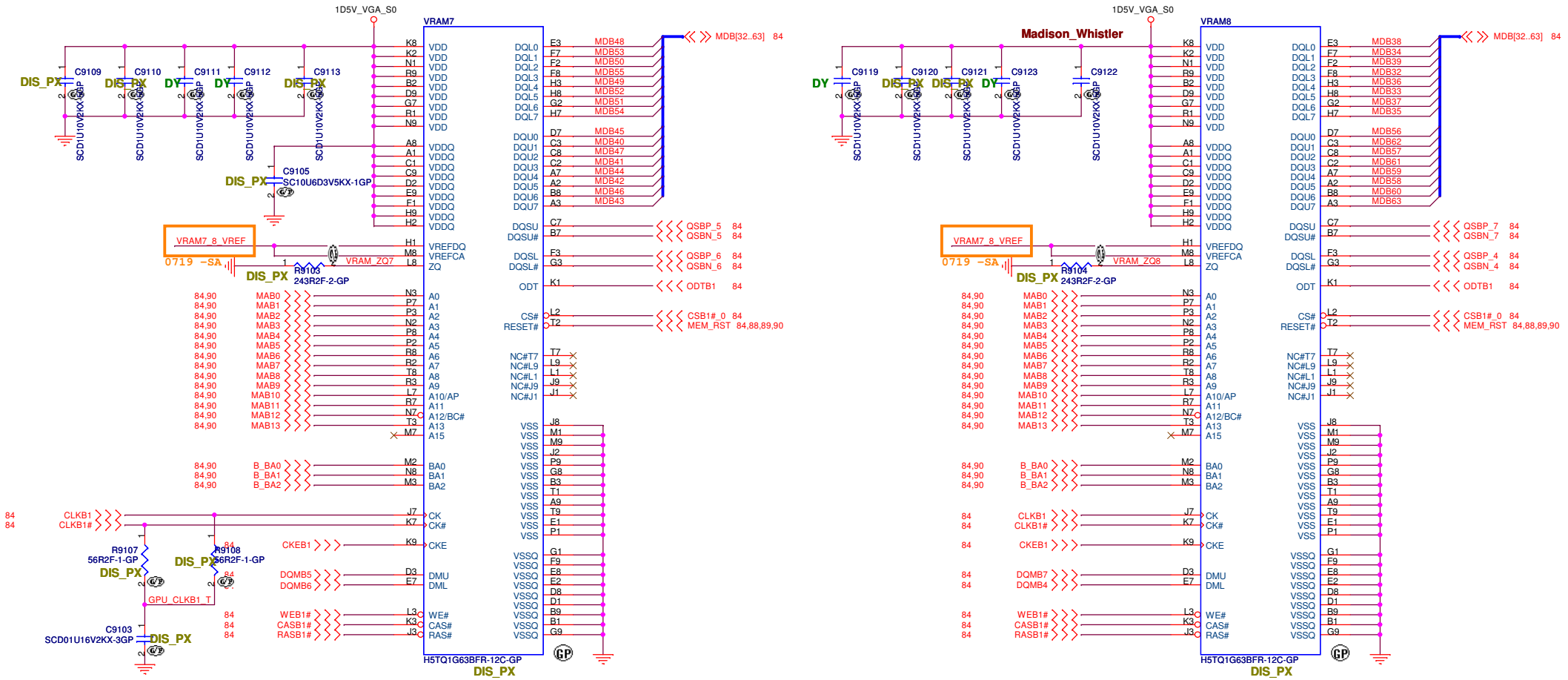

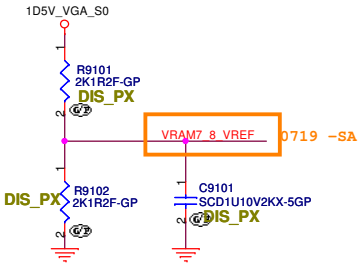

<Variant Name>

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Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
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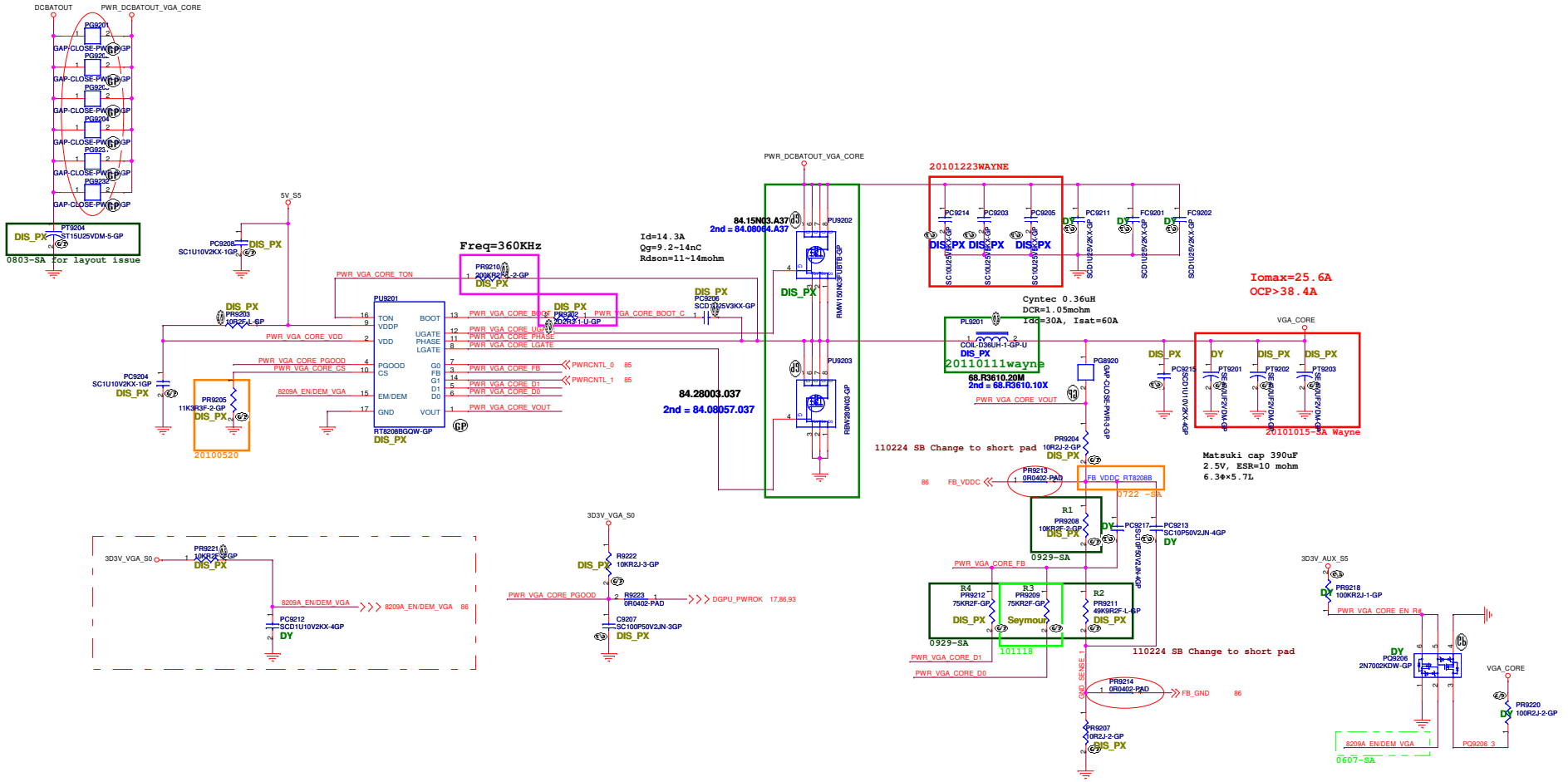
110221 SB Change to short pad



PWR_VGA_CORE_D0	PWR_VGA_CORE_D1	Level	Whistler Pro
H	L	High	1V
H	L	Medium	1V
H	H	Low	0.9V

Vout = 0.75V * [1+R1/(R2//R4)]
Vout = 0.75V * (1+R1//R2)

PWR_VGA_CORE_D0	PWR_VGA_CORE_D1	Level	Seymour XT
L	L	High	1.1V
L	H		
H	L	Medium	1V
H	H	Low	0.9V

Field side feedback 3D mark,D2D low % error
Increase voltage to 1.15V for suffer weak VGA
1008-SA

Vout = 0.75V * [1+R1/(R2//R3//R4)]
Vout = 0.75V * [1+R1/(R2//R4)]
Vout = 0.75V * (1+R1//R2)

<Variant Name>

緯創資通 Wistron Corporation
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Title: RT8208B +VGA_CORE

Size	Document Number	Rev
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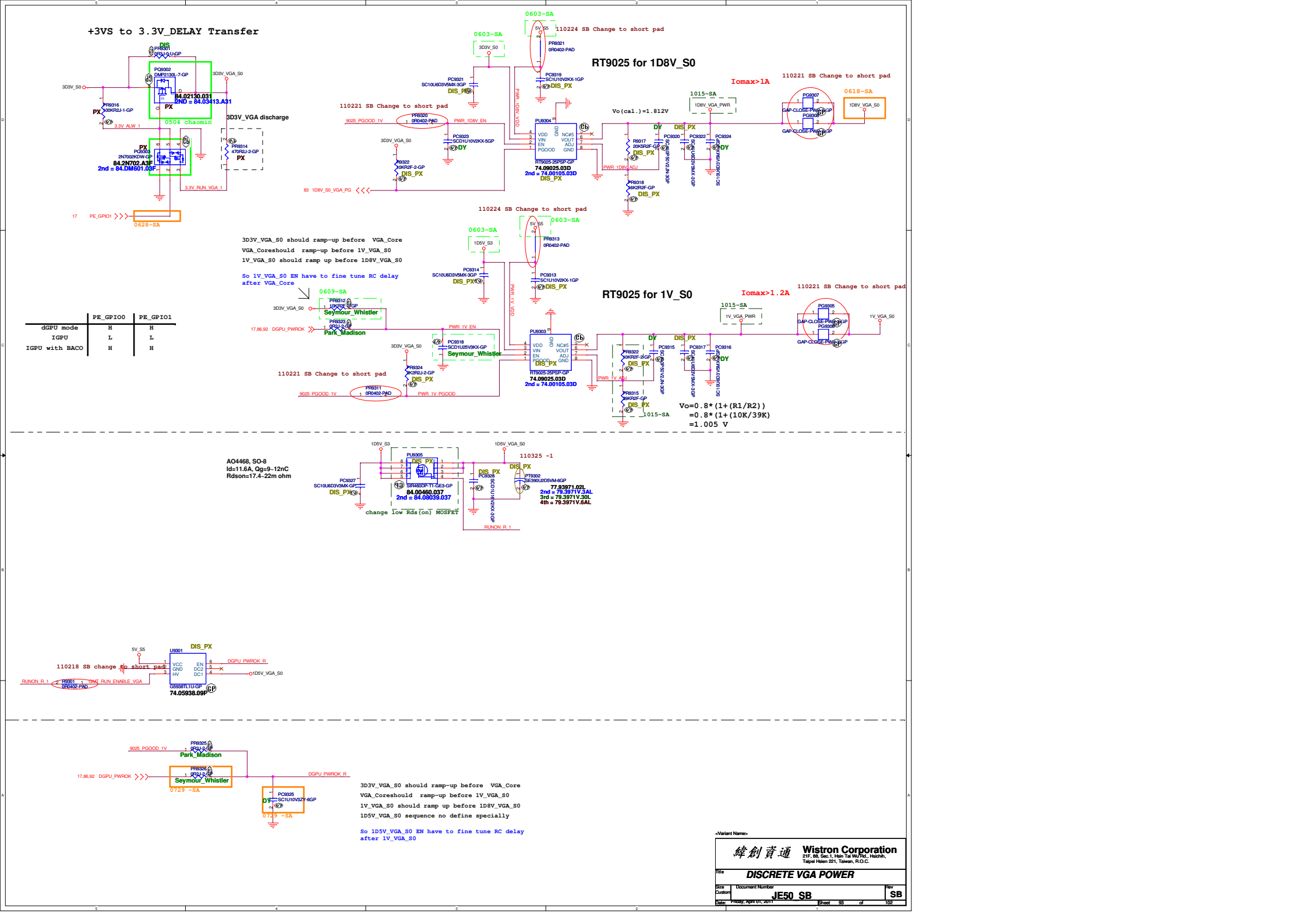
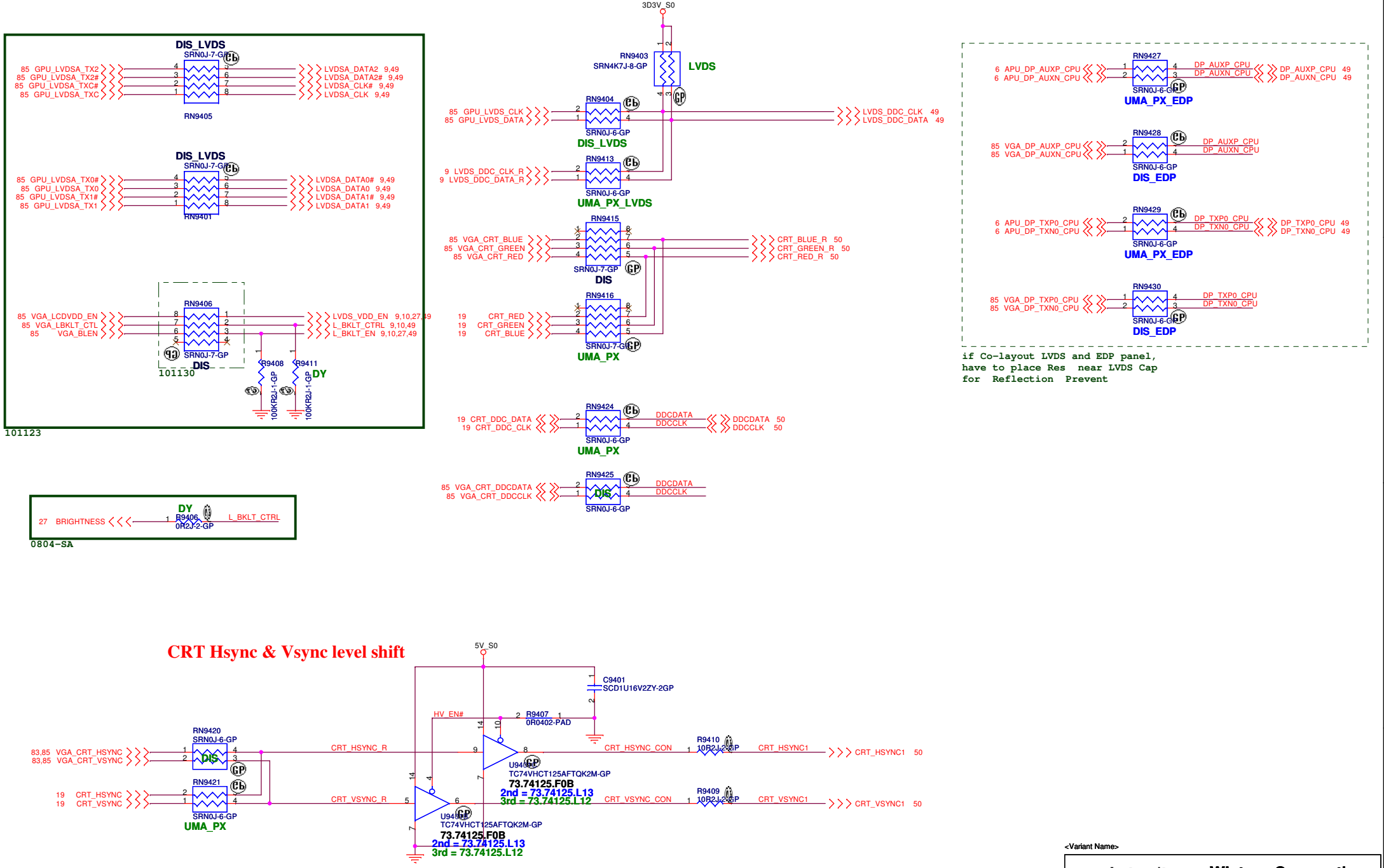


	PE_GPIO0	PE_GPIO1
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LVDS_Switch***
Size: A3	Document Number: **JE50_SB**
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Date: Friday, April 01, 2011	Sheet 94 of 102

(Blanking)

<Variant Name>

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Title

Reserved

Size	Document Number	Rev
A	JE50_SB	SB

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(Blanking)

<Variant Name>

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Title: ***Reserved***

Size	Document Number	Rev
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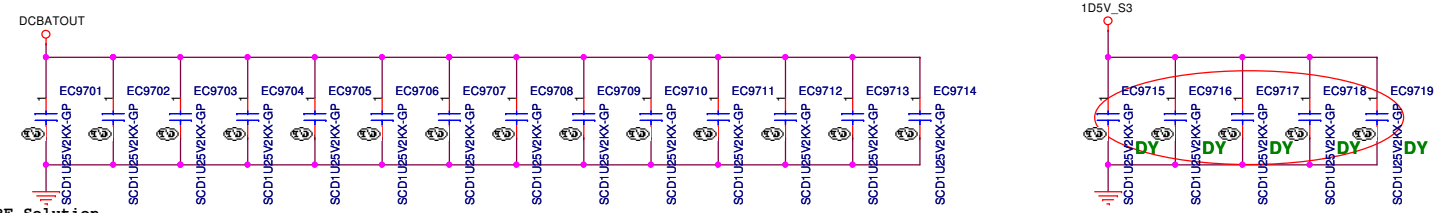
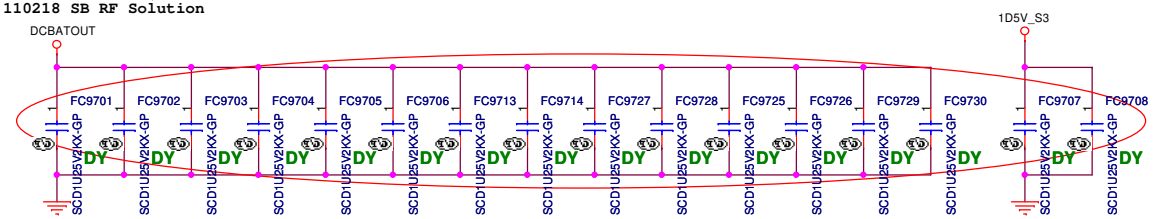
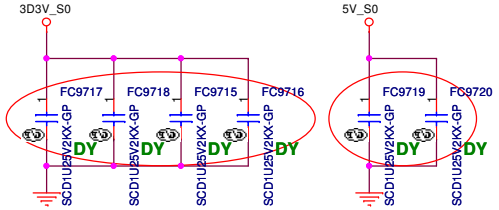
110223 SB RF Solution

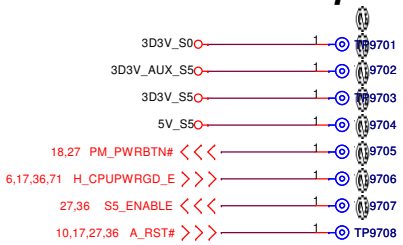


110218 SB RF Solution

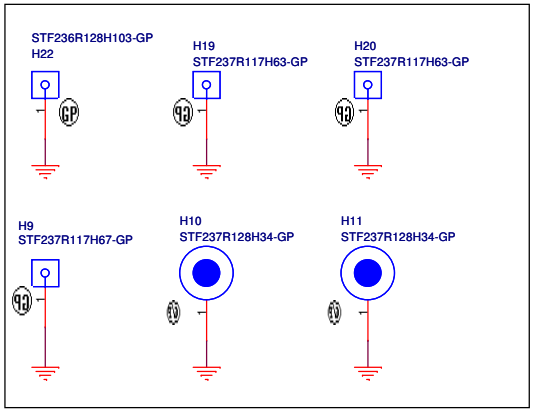




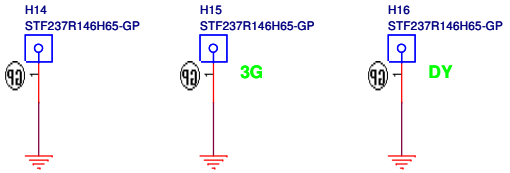
Check test point



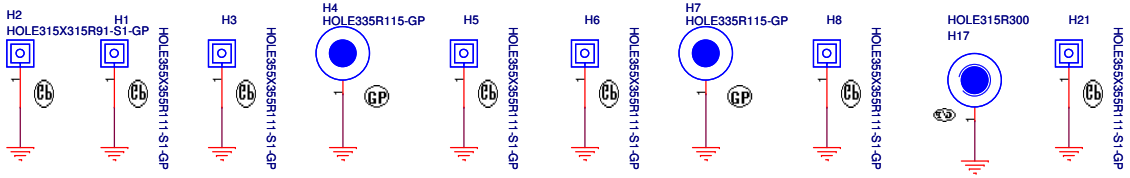
Test Point放在Dimm Door打開可量測處



SYSTEM THERMAL



WLAN WWAN



<Core Design>

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Title: UNUSED PARTS/CAP

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Modify list

65 W: PR4007 -> 187K(64.18735.6DL)
90 W: PR4007 -> 121K (64.12135.6DL)

UMA and PX R5114 ~ R5121   -> 604-ohm (64.60405.6DL)
Diserete -> R5114 ~ R5121-> 499-ohm(64.49905.6DL)

R8332 stuff 1K   for Mannhatton VGA
      stuff 5.1K(64.51015.6DL) for Vancouver VGA

if use LVDS L8711,L8709 stuff 0-ohm 0603
if use LVDS L8701,L8708 stuff bead 0603

if use EDP L8711,L8709 stuff bead 0603 ohm
if use EDP L8701,L8708 stuff 0-ohm 0603

<Core Design>

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Title: Change History

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POWER SEQUENCE

<Core Design>

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Title: POWER SEQUENCE

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<Core Design>

緯創資通

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Title

Power Block Diagram

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<Core Design>

緯創資通 **Wistron Corporation**

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Title: ***SMBUS BLOCK DIAGRAM***

Size	Document Number	Rev
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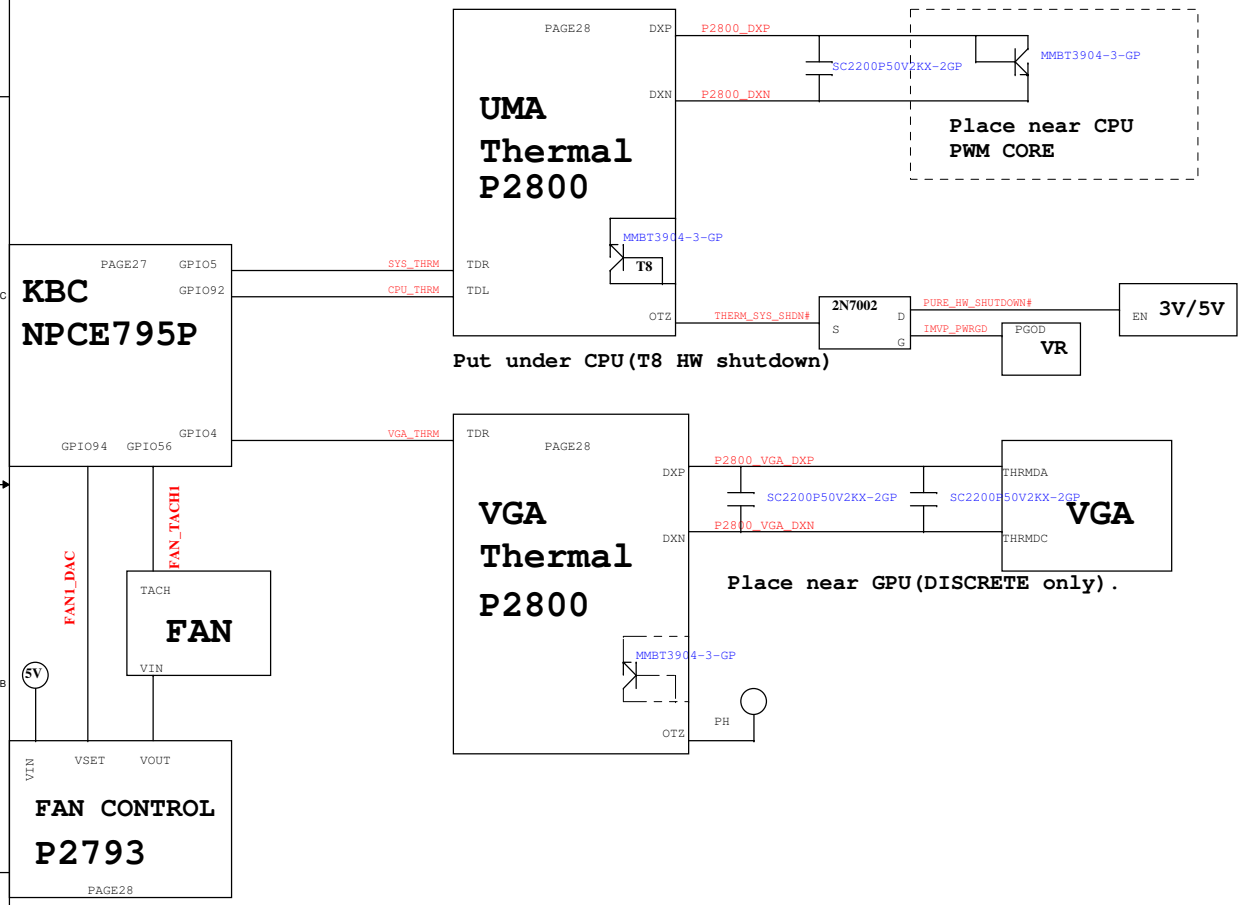
Thermal Block Diagram



Audio Block Diagram

<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	THERMAL/AUDIO BLOCK DIAGRAM
Size: Custom	Document Number: JE50_SB
Rev	SB
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